

COMPAL CONFIDENTIAL

MODEL NAME : CAZ10

PCB NO : LA-E121P

BOM P/N : 431A4231L01

Steamboat 12" AR

Kabylake U

2016-04-25

REV : 0.1 (X00)

@ : Nopop Component

EMI@ : EMI Component

@EMI@ : EMI Nopop Component

ESD@ : ESDComponent

@ESD@ : ESD Nopop Component

RF@ : RF Component

@RF@ : RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

ESPI@ : ESPI interface Component

LPC@ : External ESPI Component (SHD)

MB PCB	
Part Number	Description
DAB00186000	PCB 1S5 LA-E121P REV0 MB AR 1

Layout Dell logo



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REV:X00
PWB:

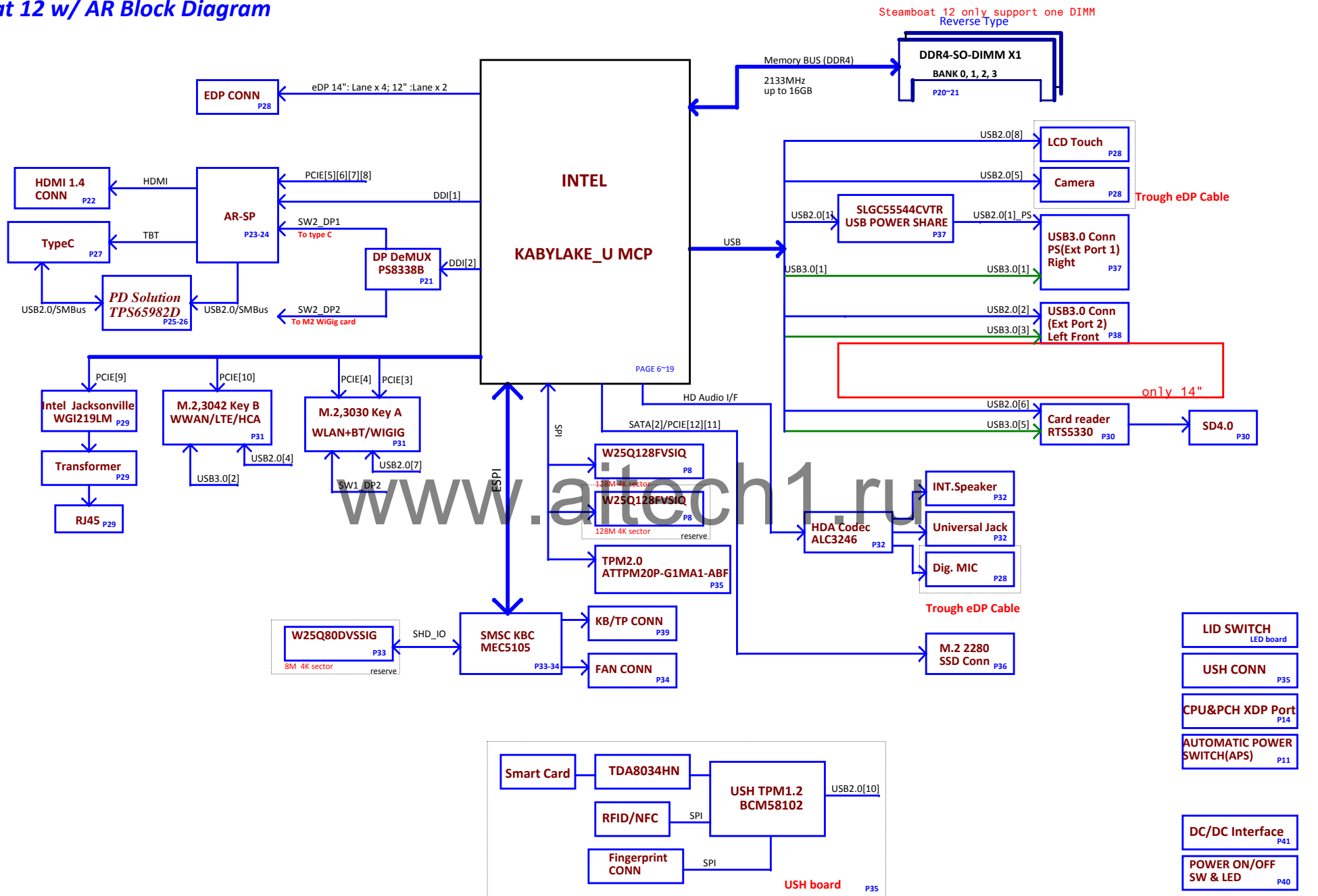
Power CKT : 0425

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Steamboat 12 w/ AR Block Diagram



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Block diagram

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

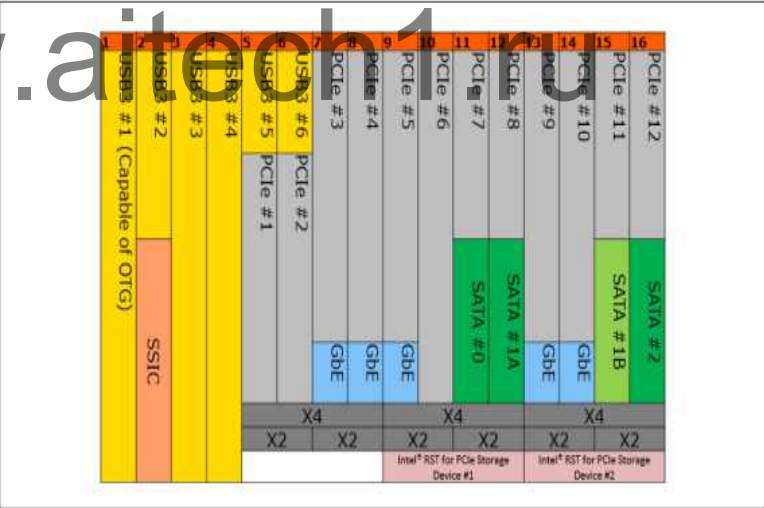
AR config

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Left Front
USB3.0-4				JUSB3-->Left Rear (SB14 only)
USB3.0-5		PCIE-1		Card Reader
USB3.0-6		PCIE-2		NA
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		M.2 3030(WIGIG)
		PCIE-5		Alpine Ridge - SP
		PCIE-6		
		PCIE-7	SATA-0	
		PCIE-8	SATA-1	
		PCIE-9		LOM
		PCIE-10		M.2 3042(HCA)
		PCIE-11	SATA-1*	M.2 2280 SSD (PCIex2 or SATA)
		PCIE-12	SATA-2	

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Left Front
3	JUSB3-->Left Rear (SB14 only)
4	M2 3042(WWAN)
5	Camera
6	Card Reader
7	M.2 3030(BT)
8	Touch Screen
9	NA
10	USH

12" not support USB3

High Speed I/O (HSIO) Lane Multiplexing in KBL U



Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	GA-150LL	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080 or1086	2.75
2	GND/PWR		Copper foil	0.5oz	0.60
		4	Core	4mil	4.00
3	Sig 1		Copper foil	0.5oz	0.60
		4.1	Prepreg	7628HRC	7.70
4	GND/PWR		Copper foil	1.0oz	1.25
		3.8	Core	4mil	4.00
5	Sig2		Copper foil	1.0oz	1.25
		4	Prepreg	7628	7.10
6	Sig3		Copper foil	0.5oz	0.60
		3.8	Core	4mil	4.00
7	GND/PWR		Copper foil	0.5oz	0.60
		3.7	Prepreg	1080 or1086	2.75
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1.0mm ± 10%)				39.4	41.40000

AR use 1086PP
Non AR use 1080PP

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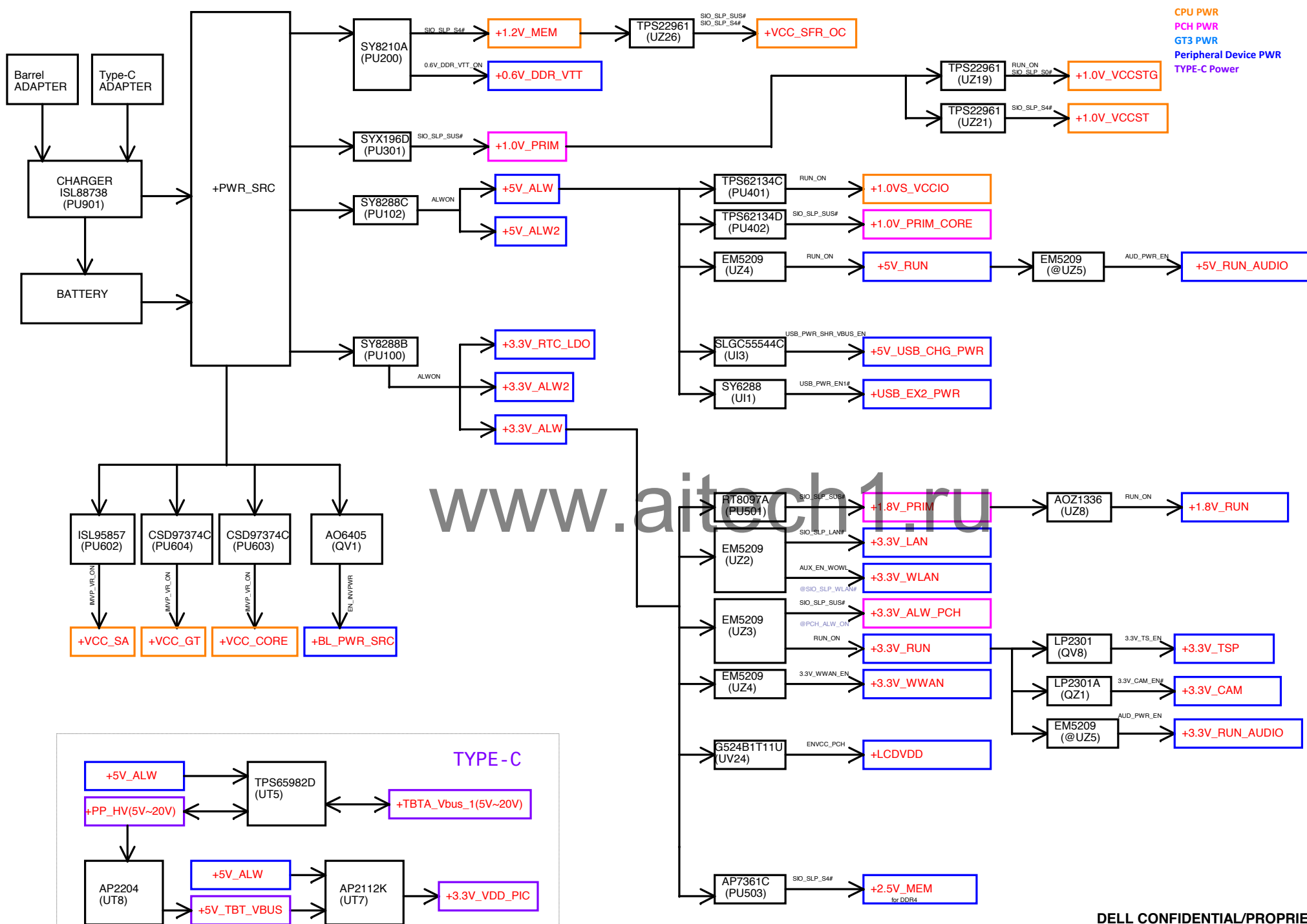
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Port assignment

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CPU PWR
PCH PWR
GT3 PWR
Peripheral Device PWR
TYPE-C Power

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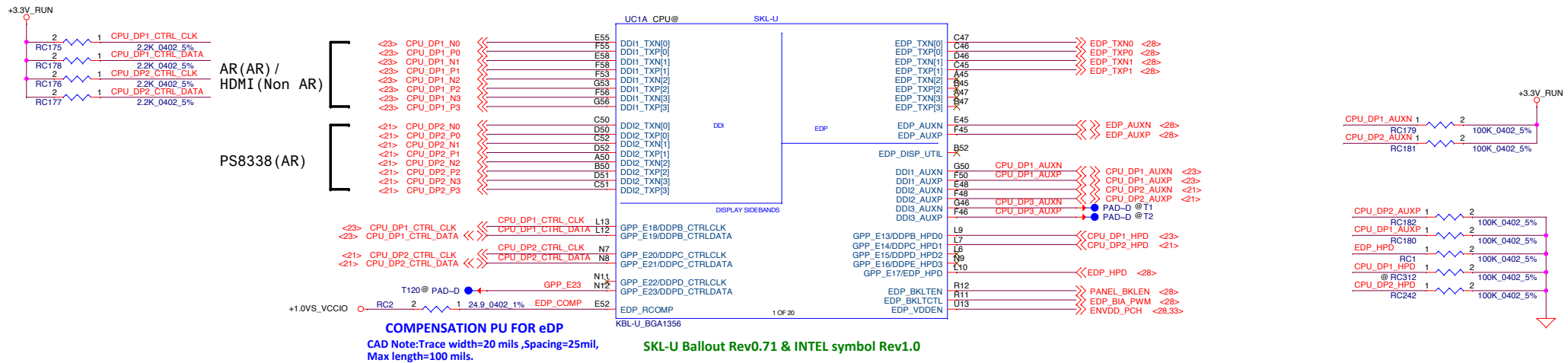
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Power rails

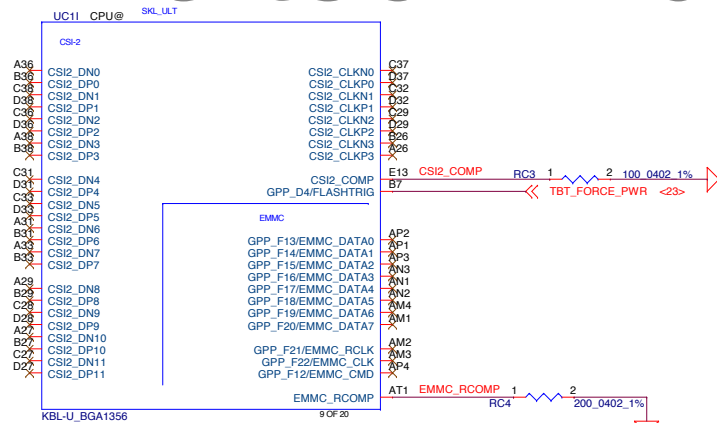
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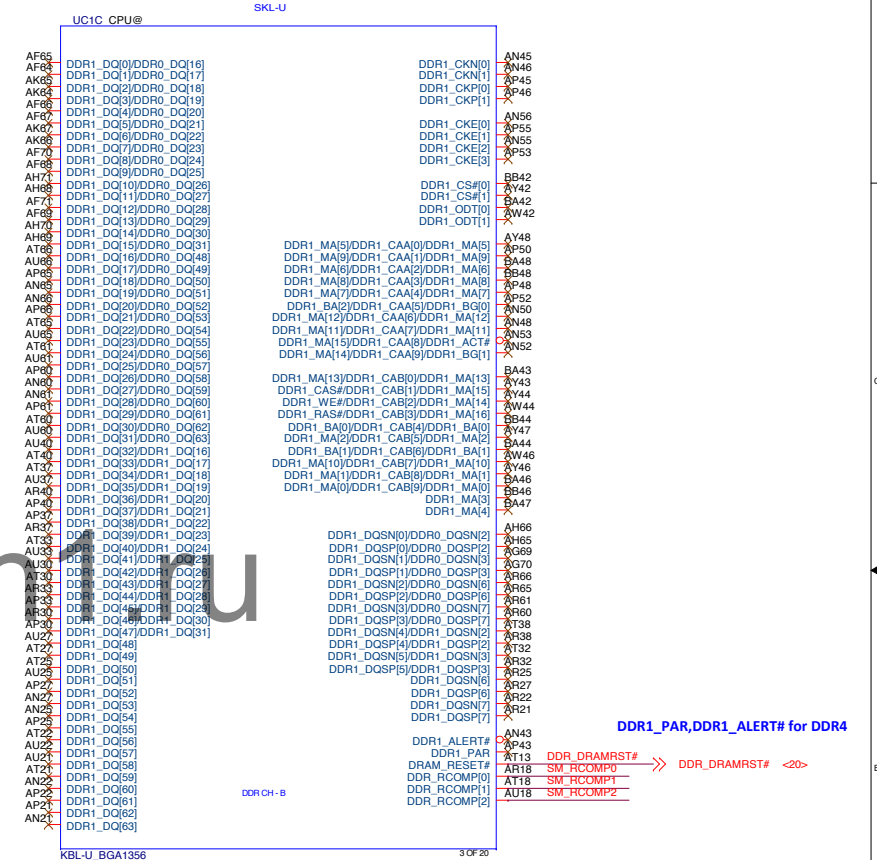
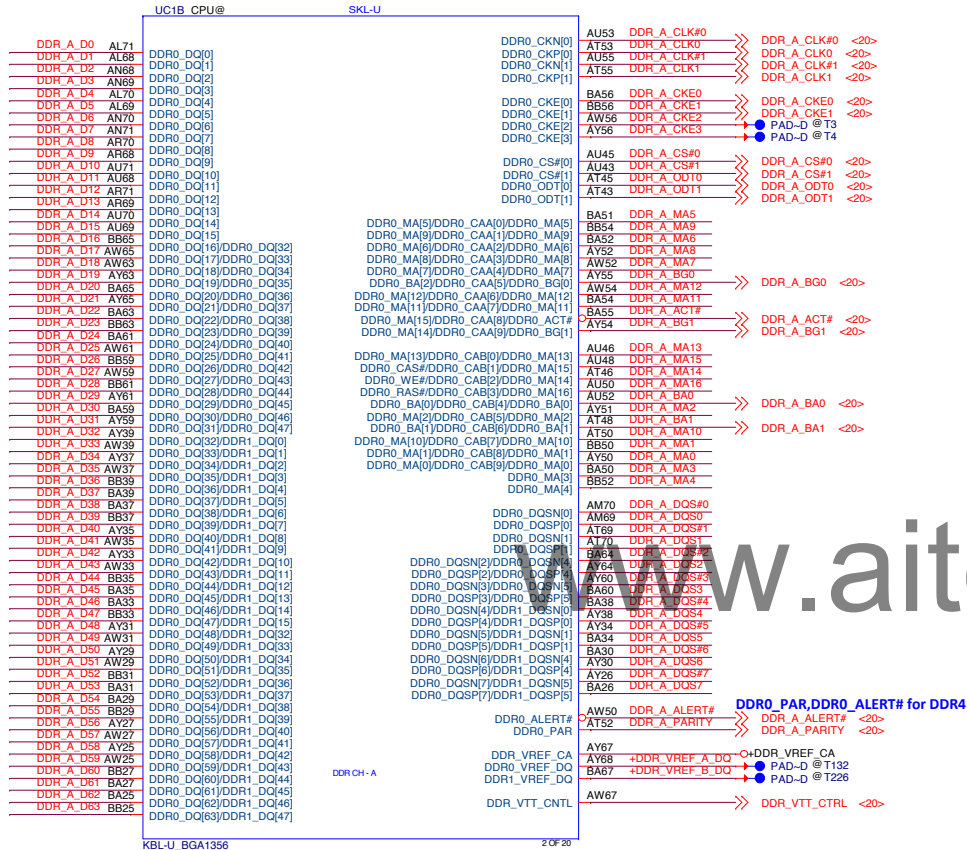


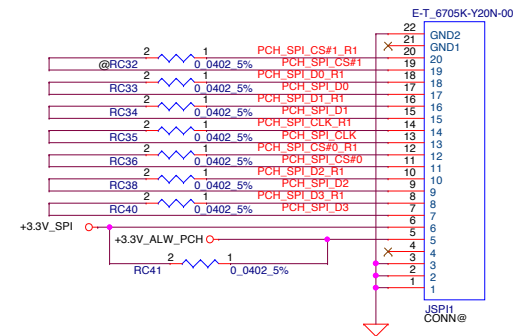
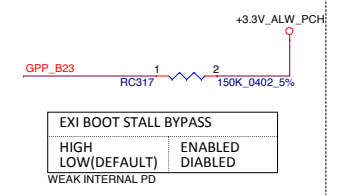
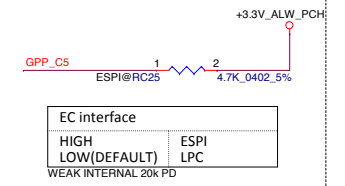
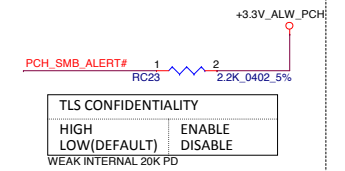
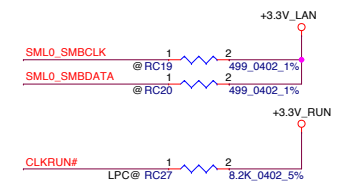
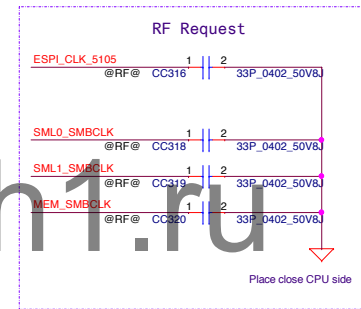
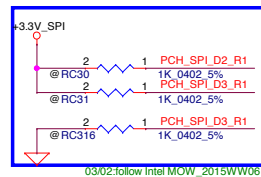
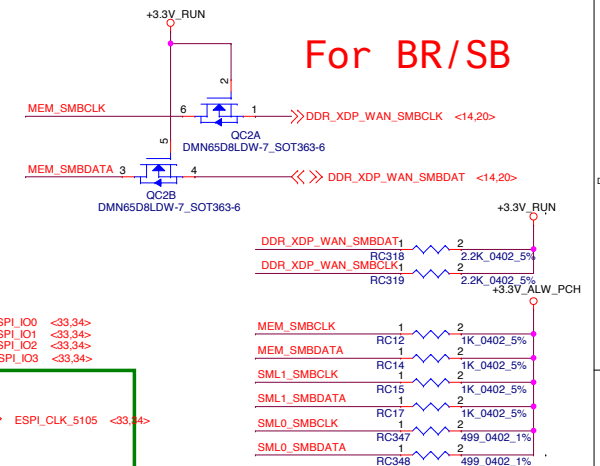
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DDR4, Ballout for side by side(Interleave)

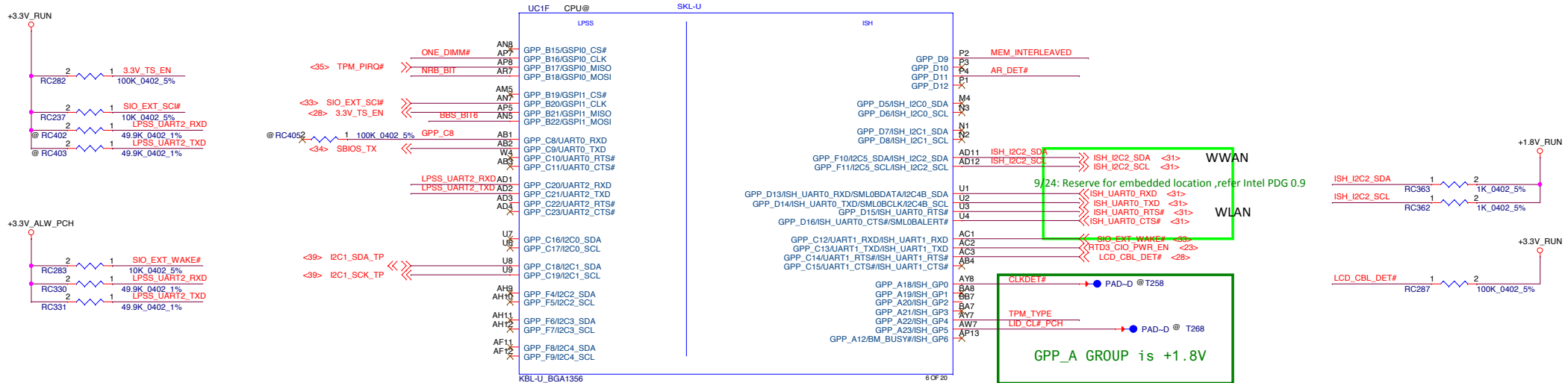
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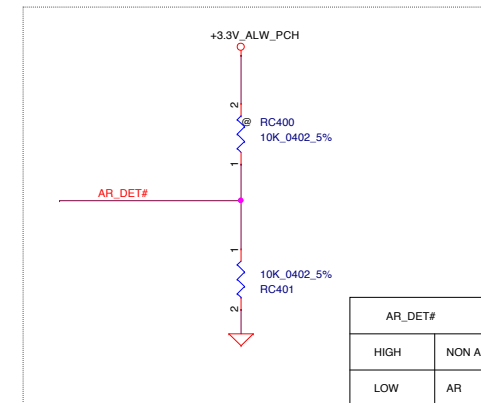
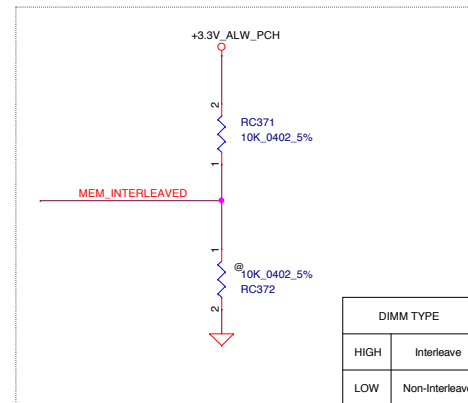
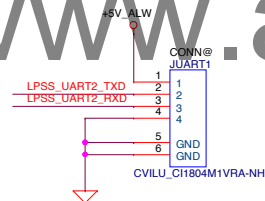
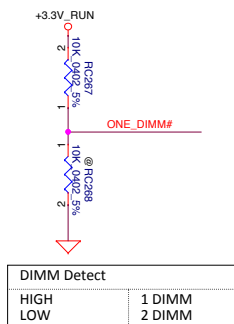
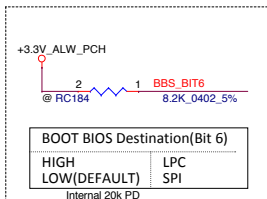
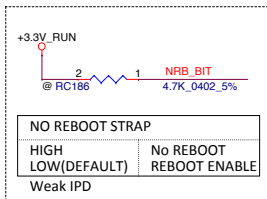
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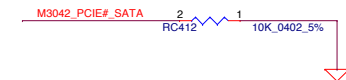
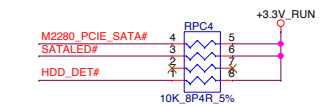
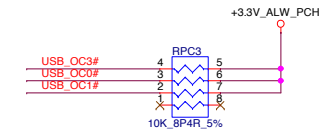
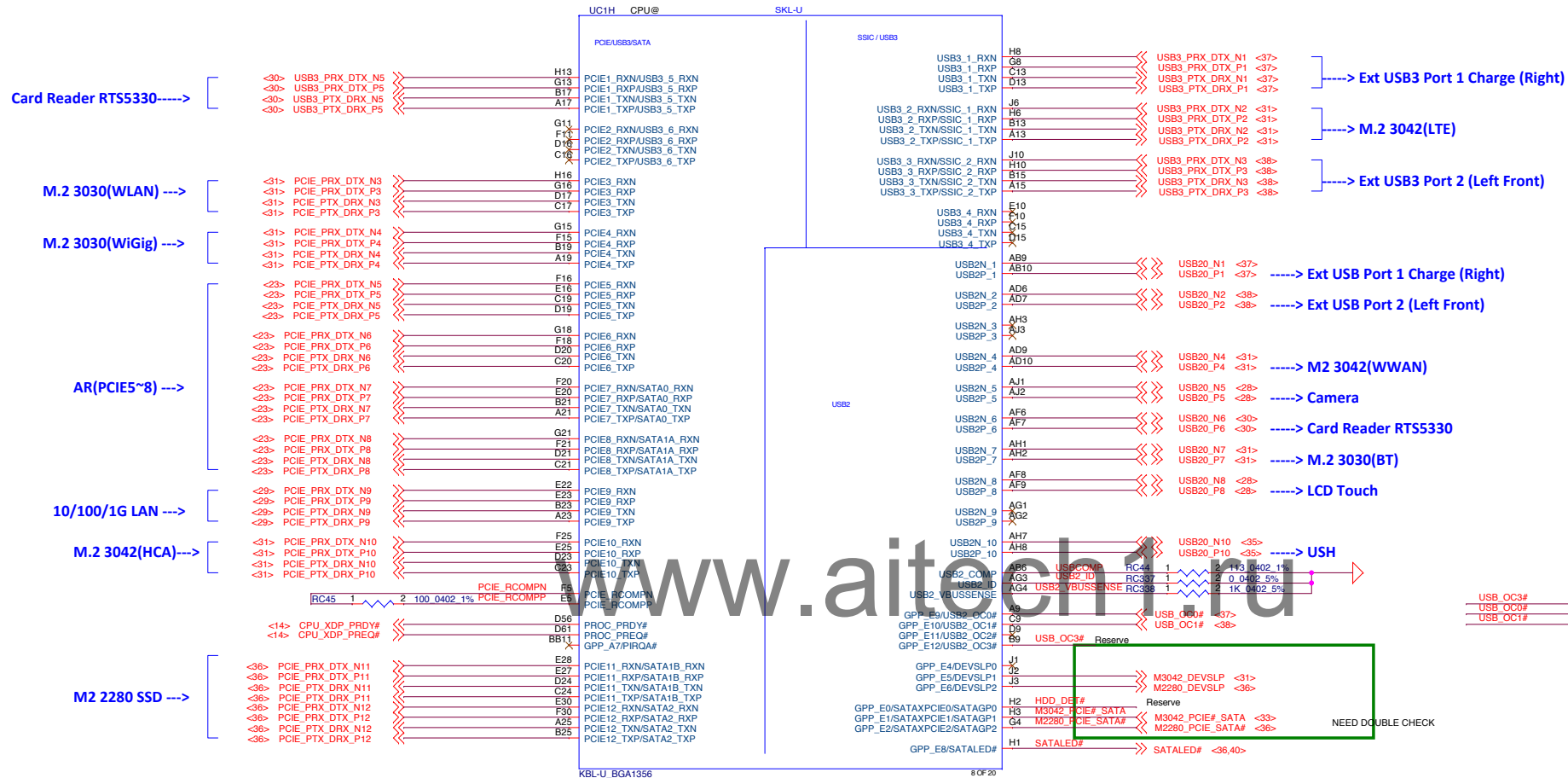
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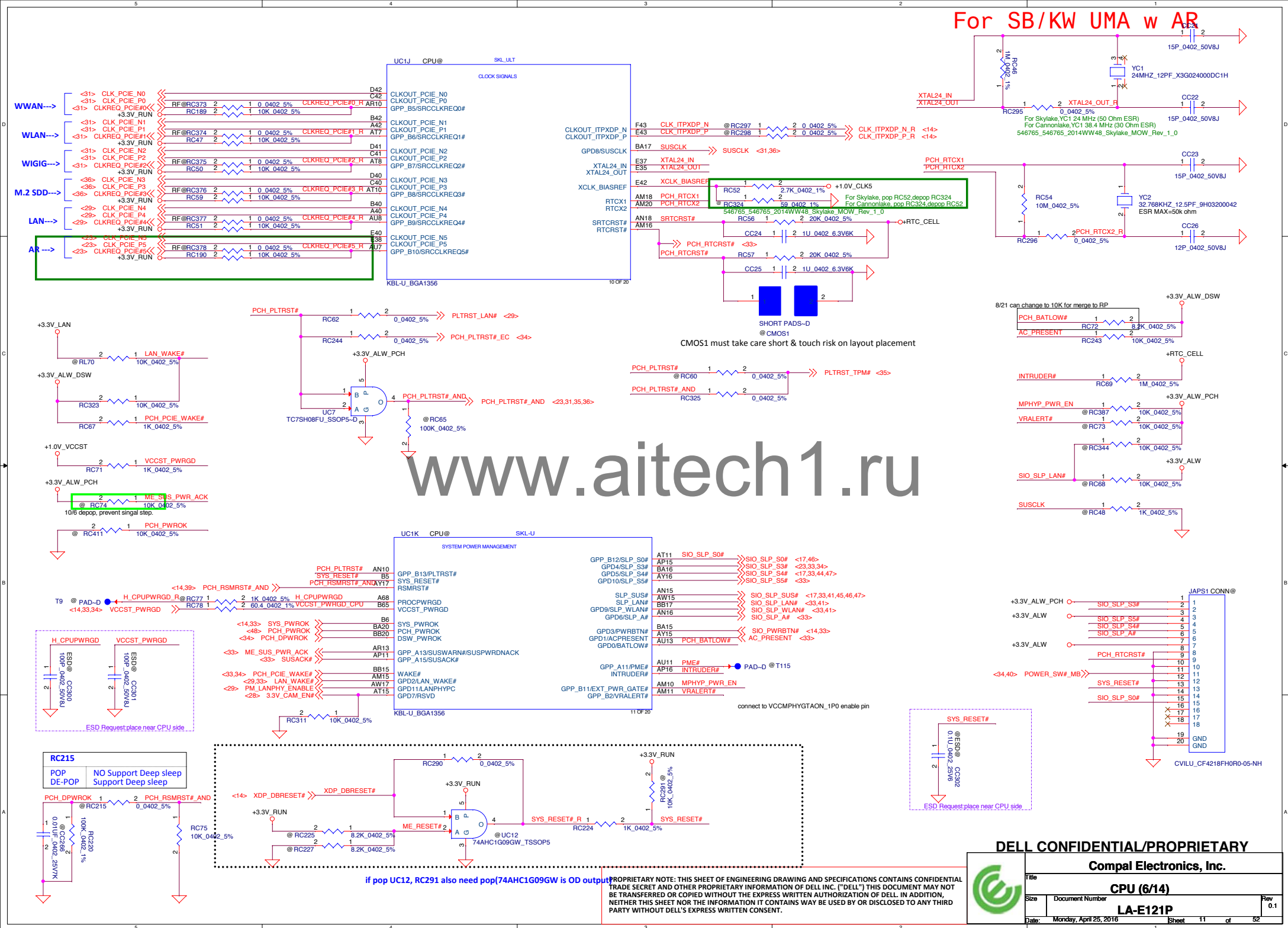
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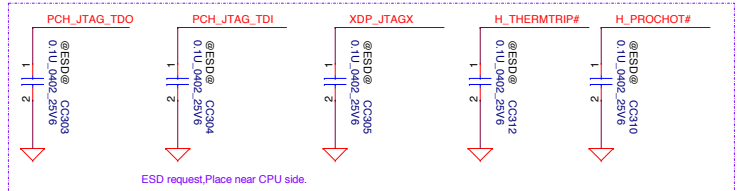
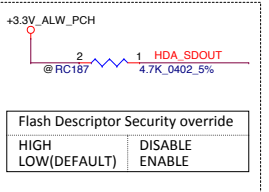
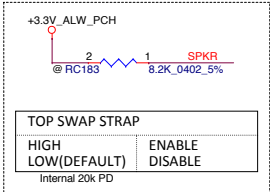
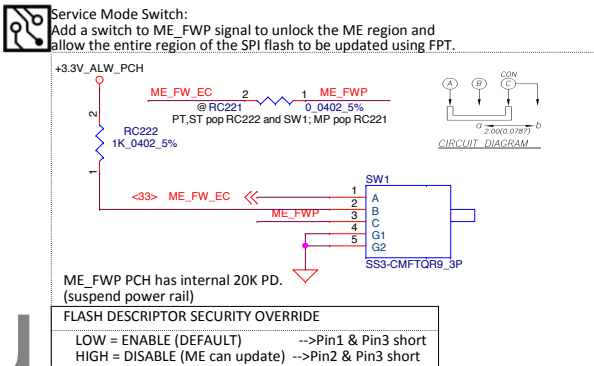
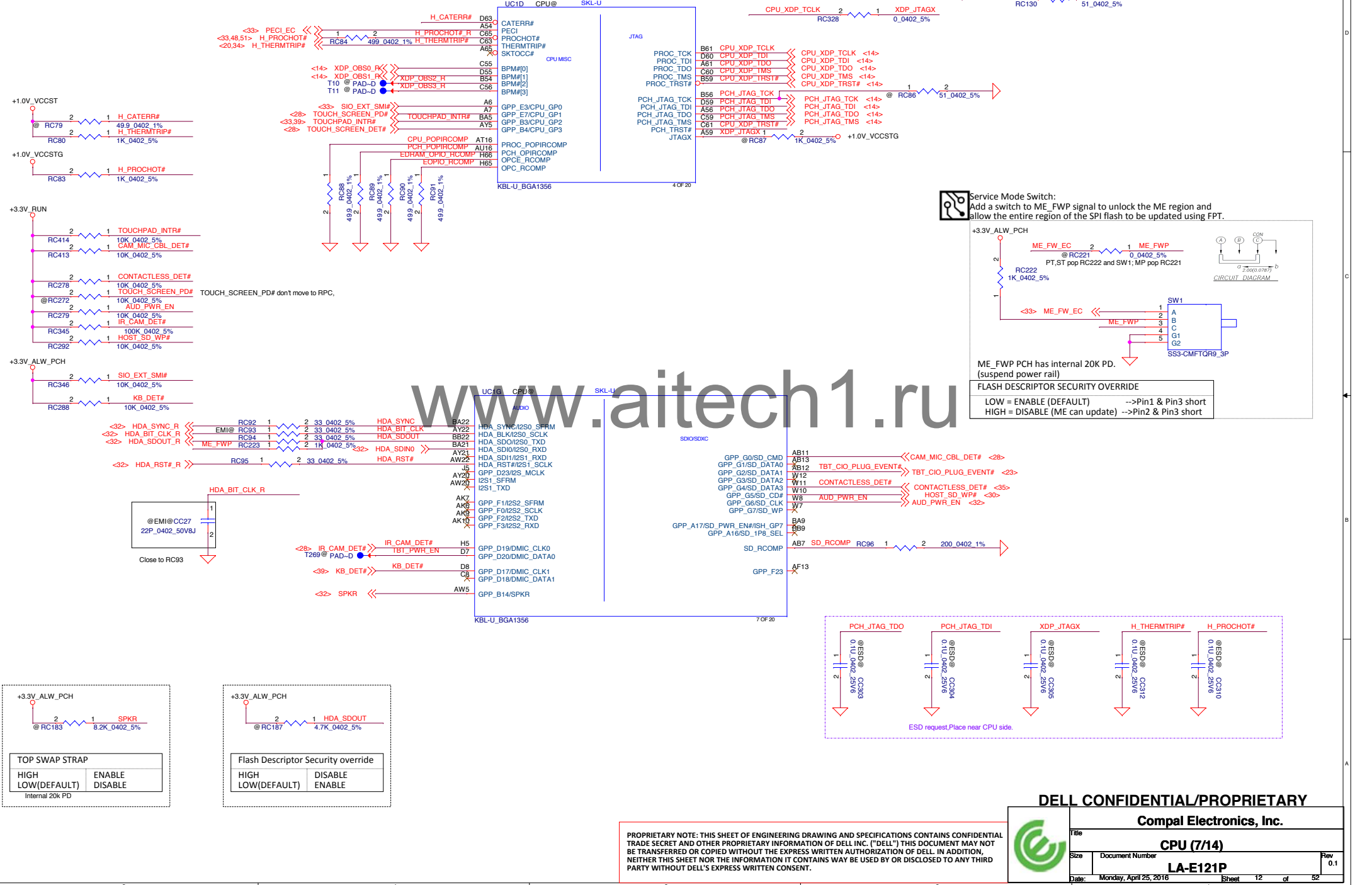
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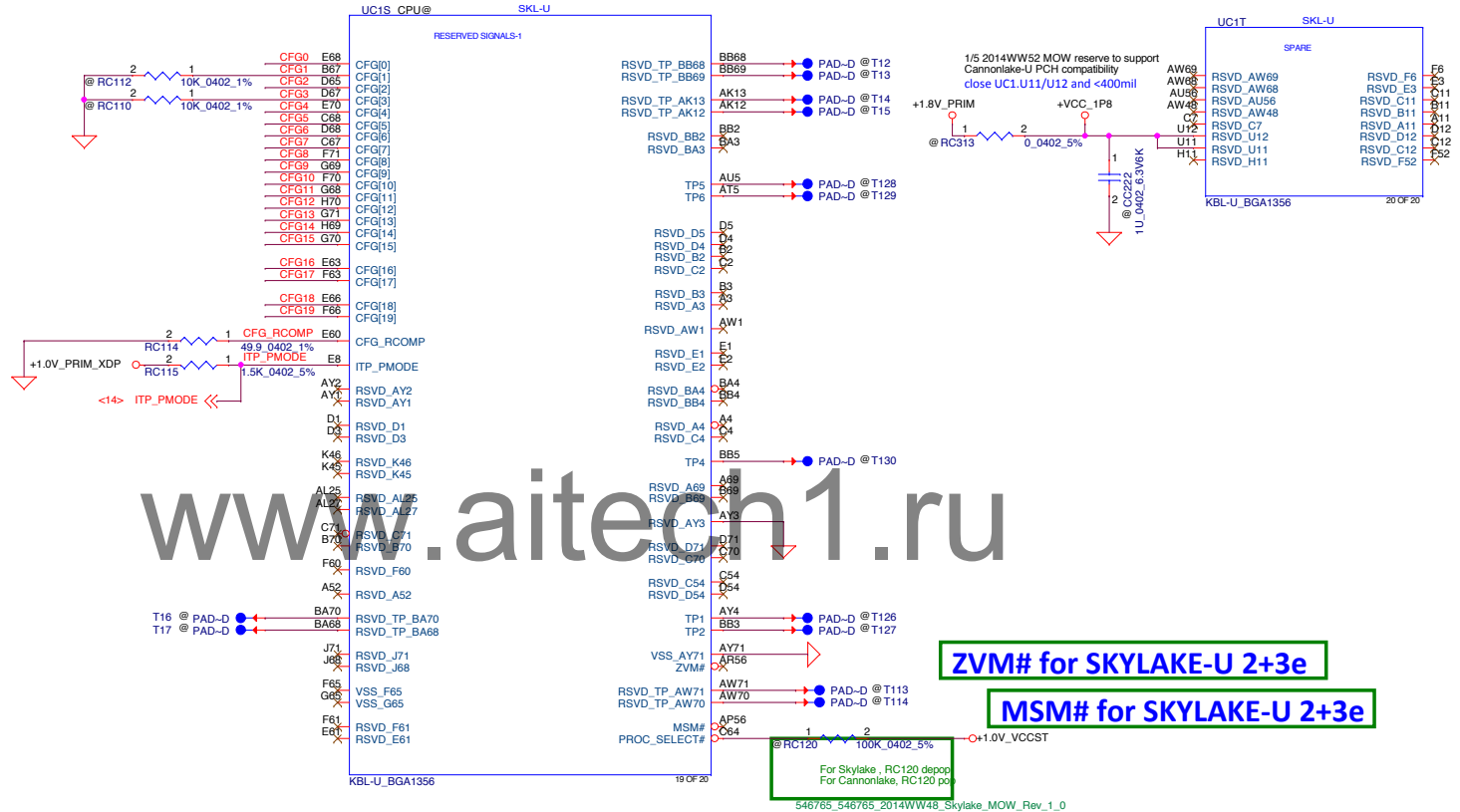
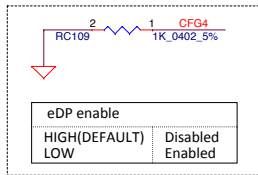
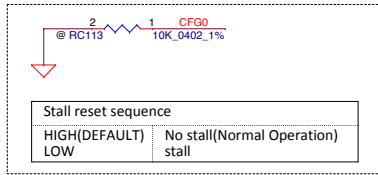
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<14> CFGQ[0..19] <<

CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin



ZVM# for SKYLAKE-U 2+3e

MSM# for SKYLAKE-U 2+3e

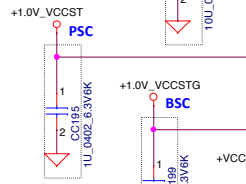
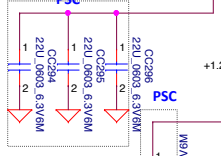
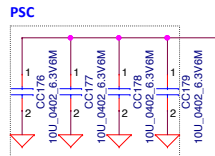
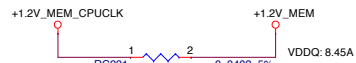
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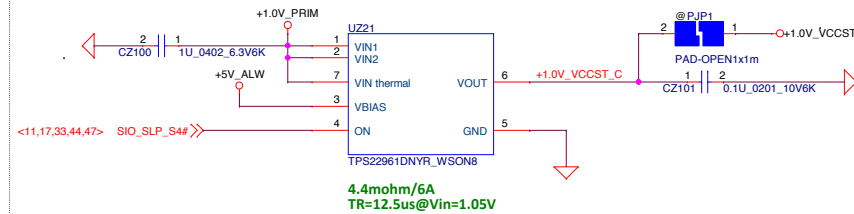


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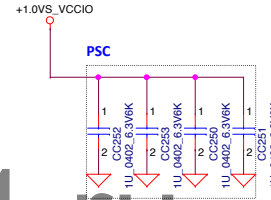
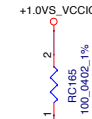
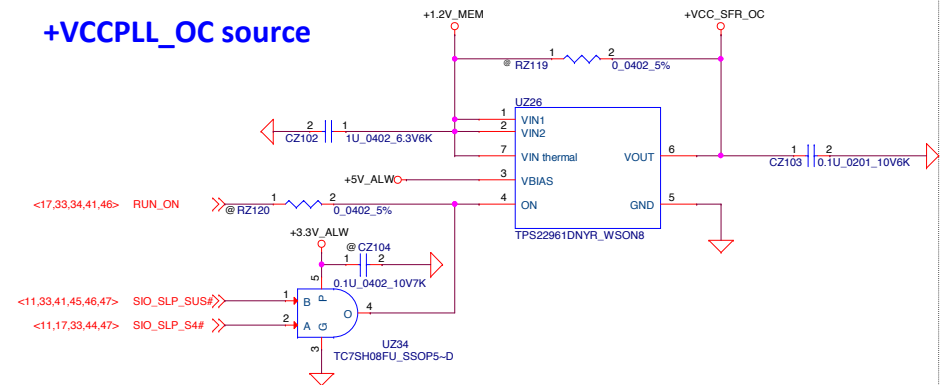
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+1.0V_VCCST source



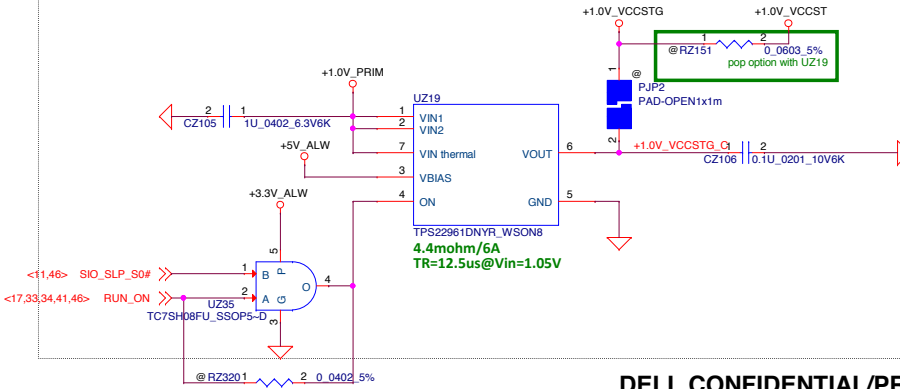
+VCCPLL_OC source



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	S0	S0k	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

+1.0V_VCCSTG source



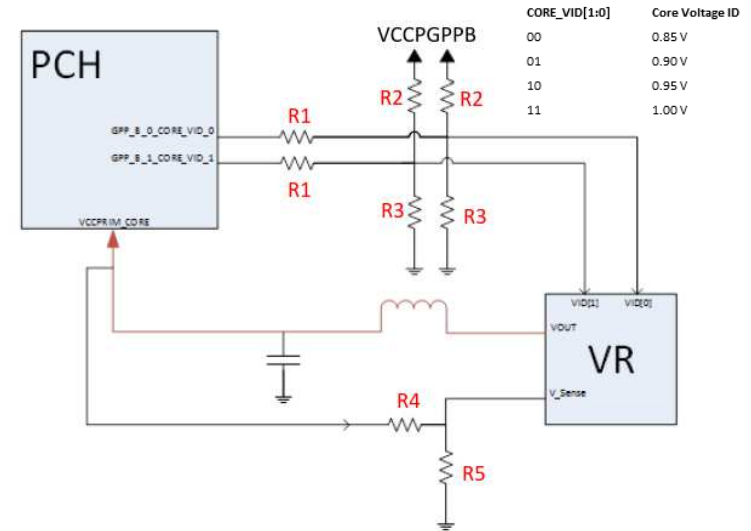
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Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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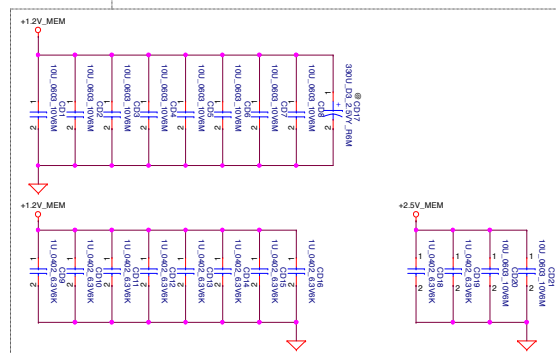


CPU (14/14)			
Title	LA-E121P		
Size	Document Number	Rev	0.1
Date:	Monday, April 25, 2016	Sheet	19 of 52

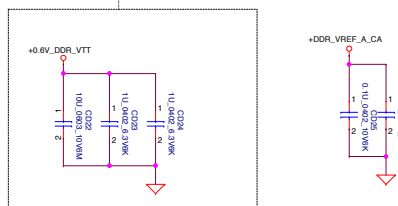
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```
<7> DDR_A_DQS#[0..7] << >>
<7> DDR_A_D[0..63] << >>
<7> DDR_A_DQS[0..7] << >>
<7> DDR_A_MA[0..16] >>
```

Layout Note:
Place near JDIMM1

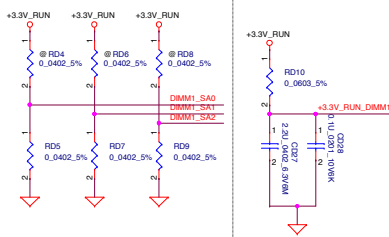


Layout Note:
Place near
JDIMM1.258



DIMM Select

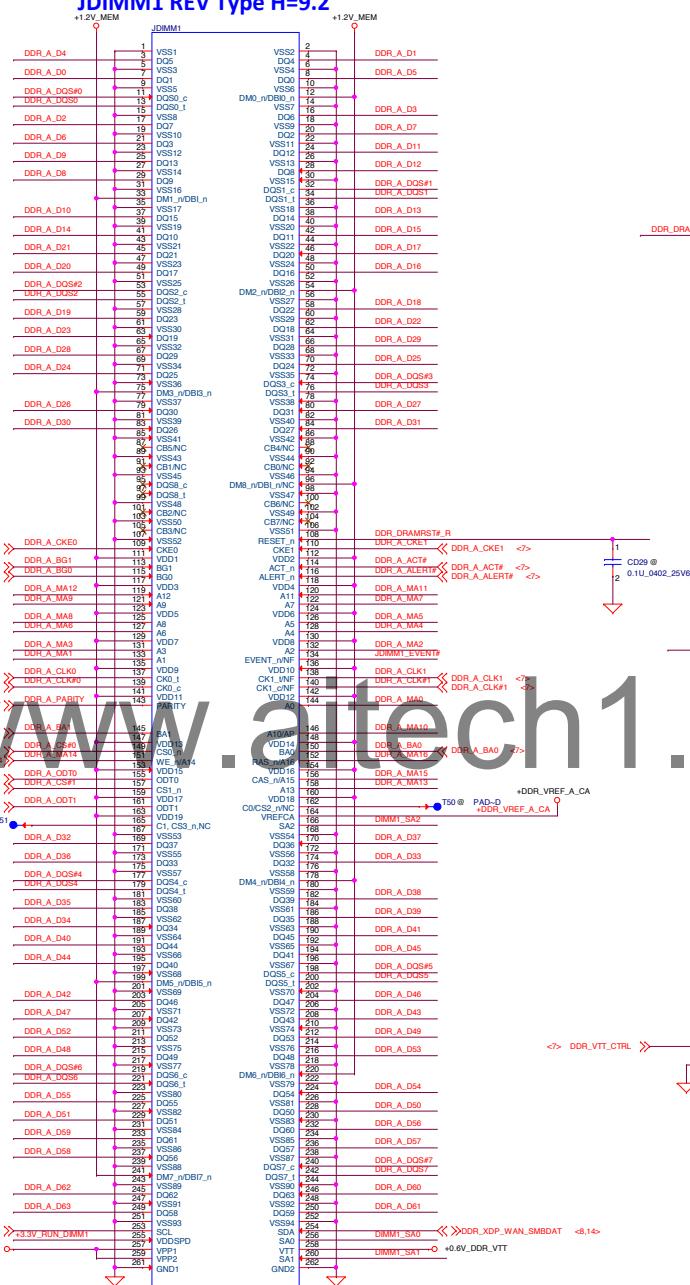
	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



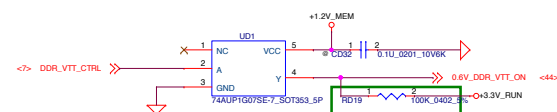
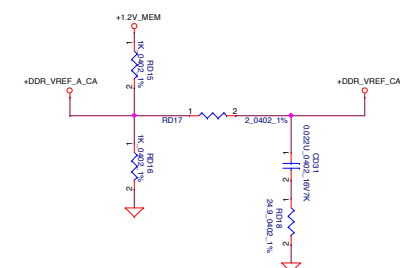
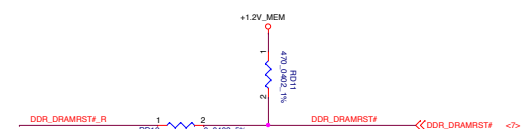
<8.14> DDR XDP W

+2.5V

JDIMM1 REV Type H=9.2



LINK SP07001D200 DONE



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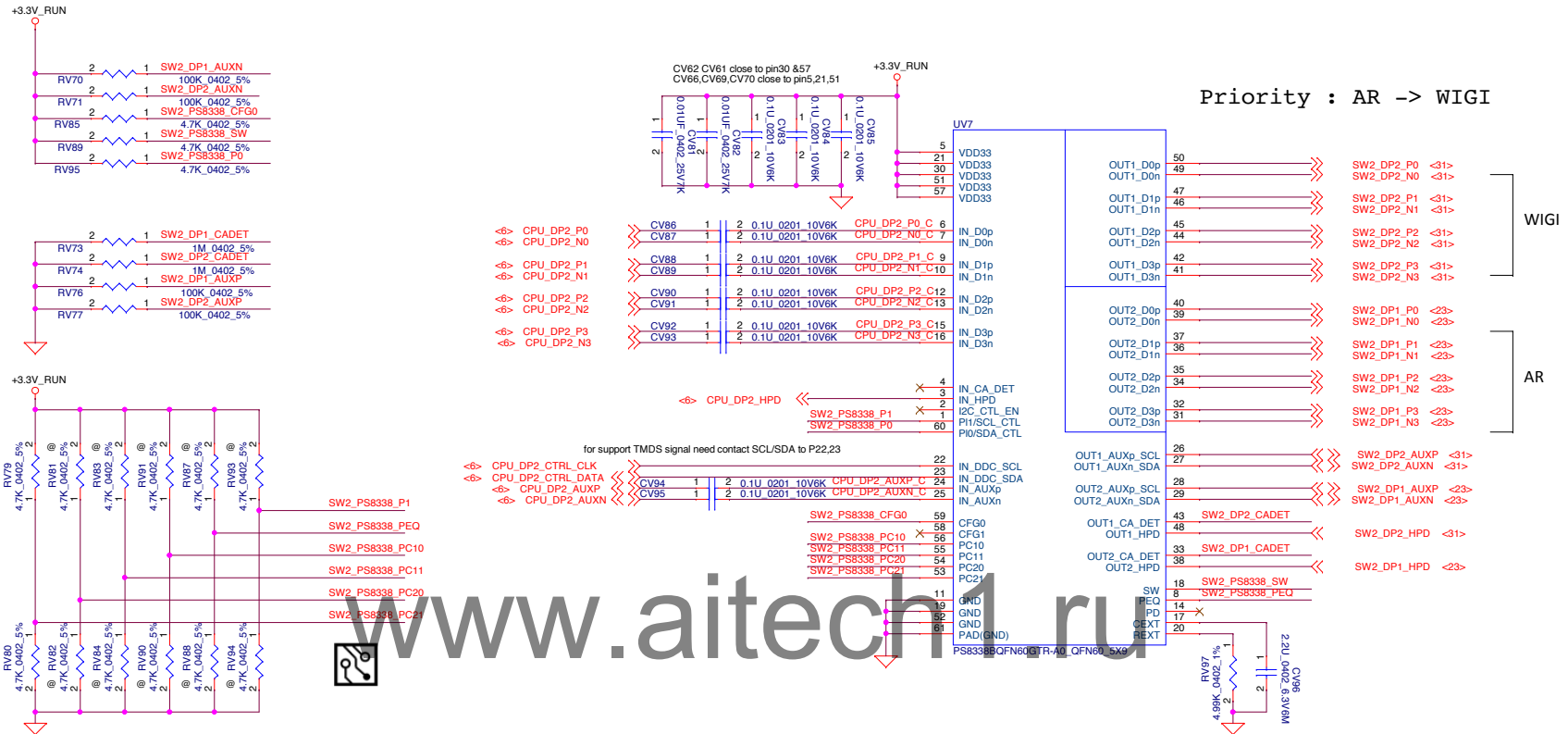
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DDR4

LA-E121P

Date: Monday, April 25, 2016 Sheet 20 of



```
Port switching control or priority configuration. Internal pull down ~150K $\Omega$ , 3.3V
I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected
For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged
SW = H: Port2 has higher priority when both ports are plugged (default)
```

vender suggest MUX use LLEQ PEQ=M and PI0=H !!

Programmable input equalization levels, Internal pull down at ~150Kohm, 3.3V I/O
 PEQ =
 L: default, LEQ, compensate channel loss up to 11.5dB @HBR2
 H: LEQ, compensate channel loss up to 14.5dB @HBR2
 M: LEQ, compensate channel loss up to 8.5dB @HBR2

P10: Automatic EQ disable, Internal pull down ~150K ohm, 3.3V I/O
P10 = L: Automatic EQ enable(default)
H: Automatic EQ disable

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DP SW2 PS8338

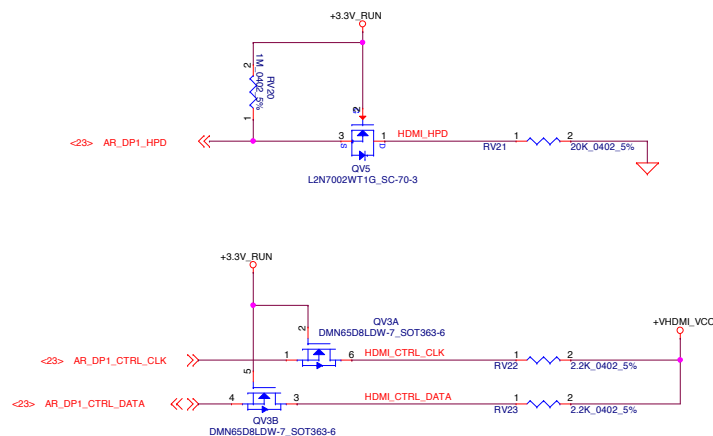
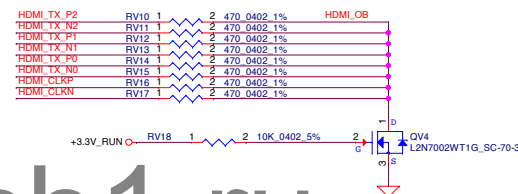
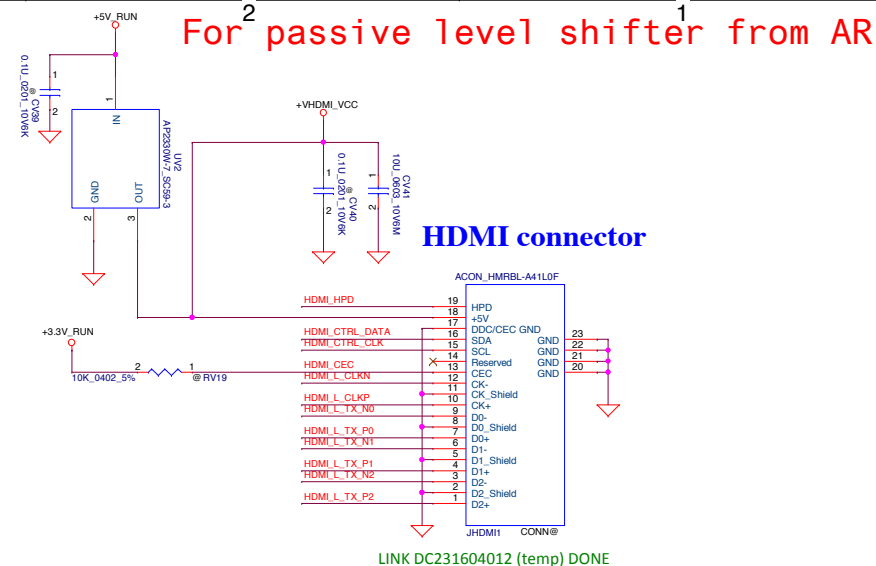
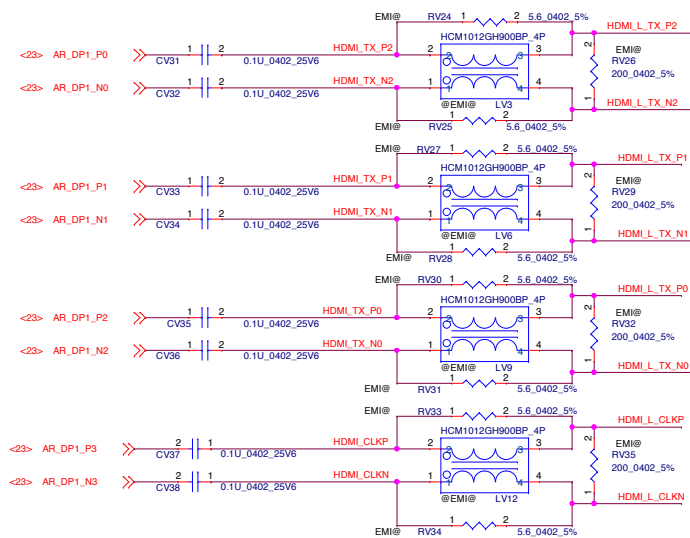
LA-E121P

Rev	
0.1	

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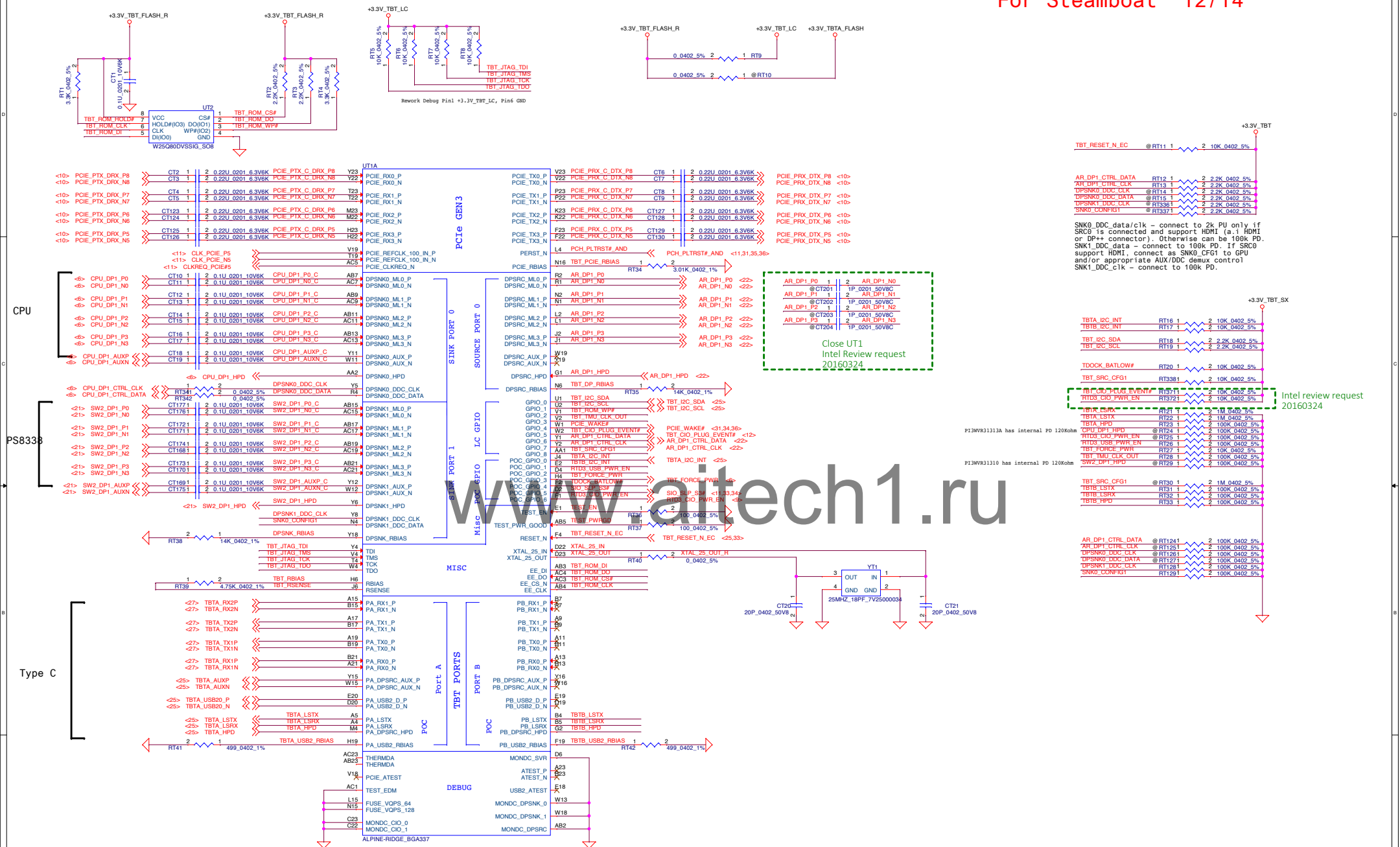
HDMI CONN

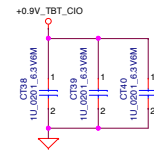
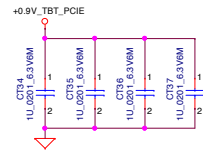
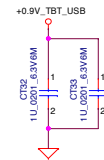
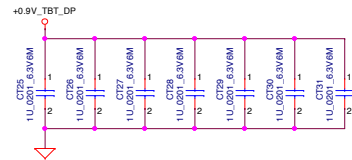
LA-E121P

Rev 0.1

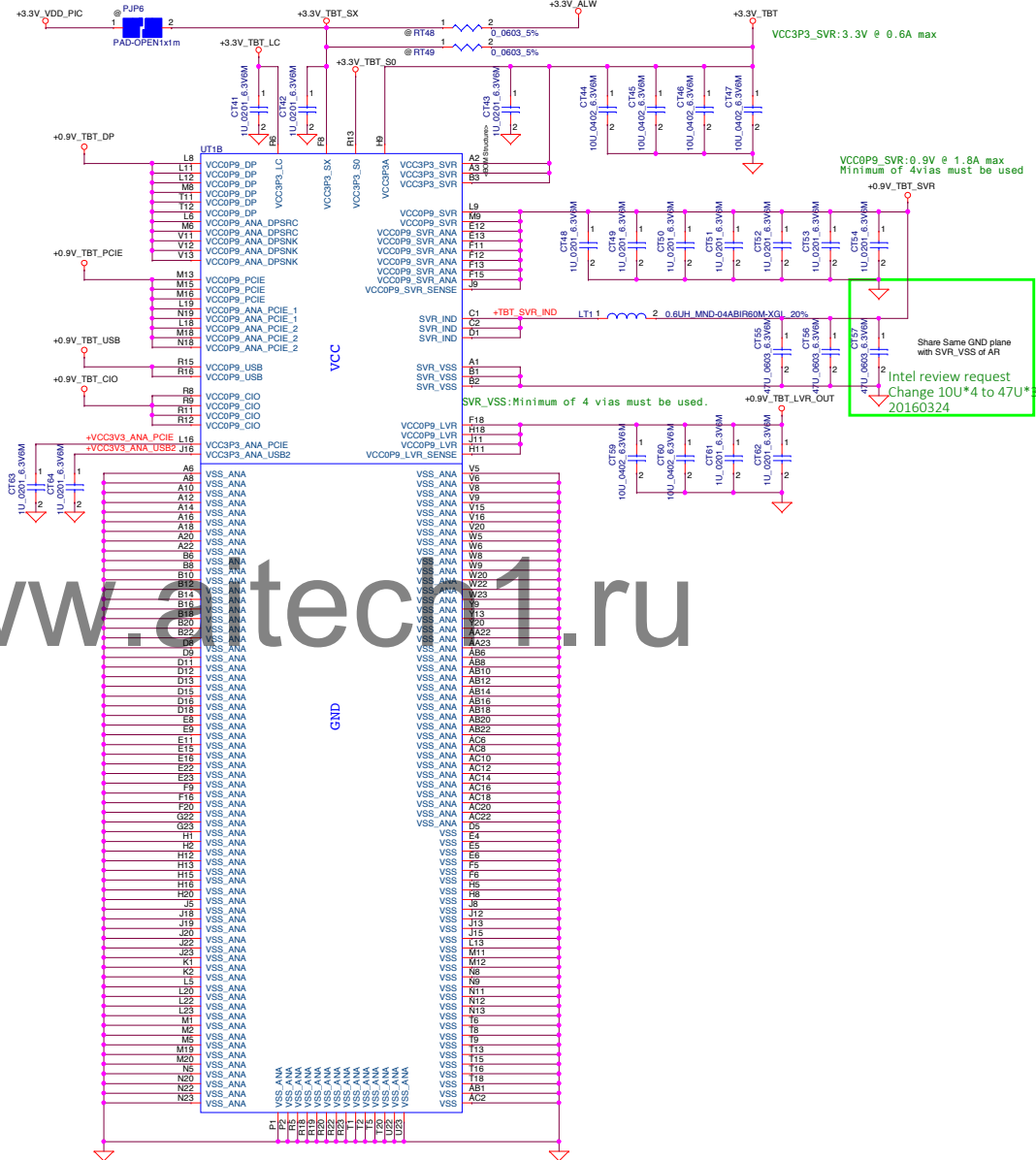
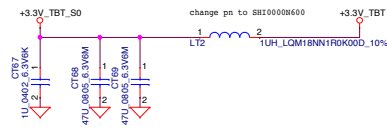
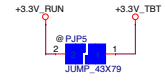
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TBT Power circuit



86	VSS_ANA	W8
88	VSS_ANA	W9
89	VSS_ANA	W10
90	VSS_ANA	W11
91	VSS_ANA	W12
92	VSS_ANA	W13
93	VSS_ANA	W14
94	VSS_ANA	W15
95	VSS_ANA	W16
96	VSS_ANA	W17
97	VSS_ANA	W18
98	VSS_ANA	W19
99	VSS_ANA	W20
100	VSS_ANA	W21
101	VSS_ANA	W22
102	VSS_ANA	W23
103	VSS_ANA	W24
104	VSS_ANA	W25
105	VSS_ANA	W26
106	VSS_ANA	W27
107	VSS_ANA	W28
108	VSS_ANA	W29
109	VSS_ANA	W30
110	VSS_ANA	W31
111	VSS_ANA	W32
112	VSS_ANA	W33
113	VSS_ANA	W34
114	VSS_ANA	W35
115	VSS_ANA	W36
116	VSS_ANA	W37
117	VSS_ANA	W38
118	VSS_ANA	W39
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122	VSS_ANA	W43
123	VSS_ANA	W44
124	VSS_ANA	W45
125	VSS_ANA	W46
126	VSS_ANA	W47
127	VSS_ANA	W48
128	VSS_ANA	W49
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201	VSS_ANA	W122
202	VSS_ANA	W123
203	VSS_ANA	W124
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206	VSS_ANA	W127

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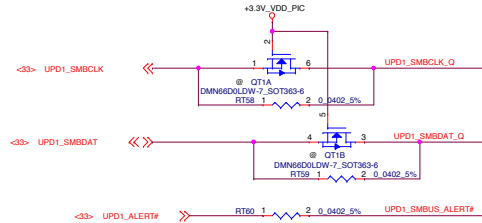
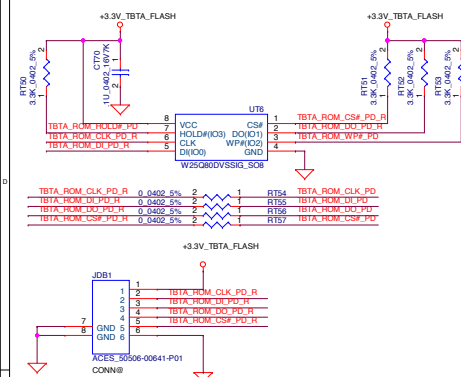
TBT-AR-SP(2/2) PWR,VSS

or
LA-E121P

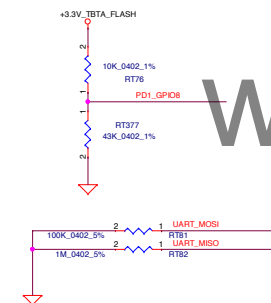
Date: Monday, April 25, 2016 Sheet 24 of 52

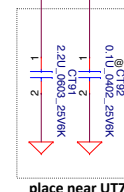
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DIV = R2 / (R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UPP only 5V @0.8A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UPP only 5V @0.8A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.20	0.28	2	UPP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UPP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.40	0.48	4	DPP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate
0.50	0.58	5	DPP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations TI VID supported Accepts power role swaps but will not initiate Accepts data role swap to UEP and can initiate
0.60	0.68	6	DPP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations TI VID supported Accepts power role swaps but will not initiate Accepts data role swap to UEP and can initiate
0.70	1.00	7	Infinite boot retry from Flash to Host IF cycles.



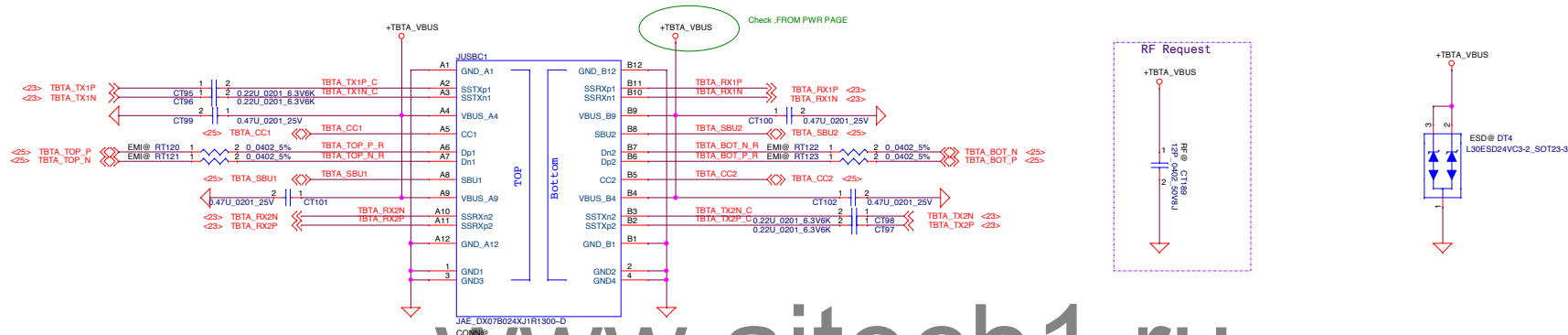


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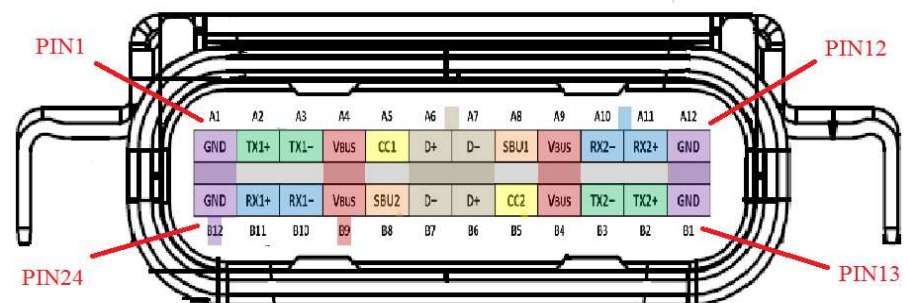
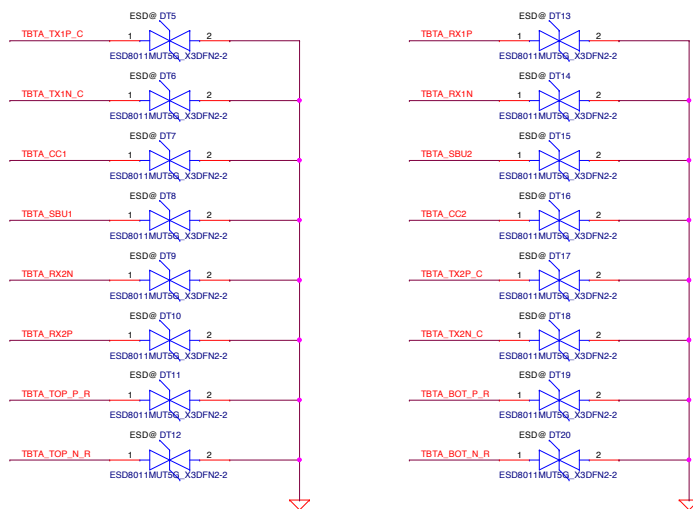
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For AR Config



Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B
Link DC23300MEBL Done



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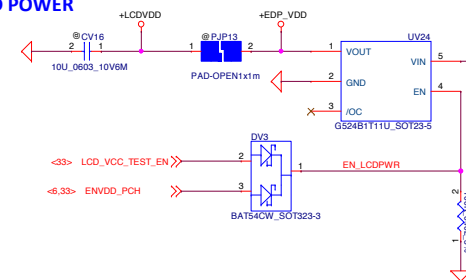


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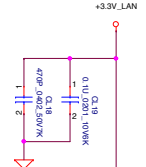
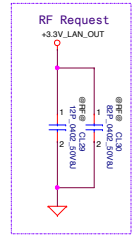
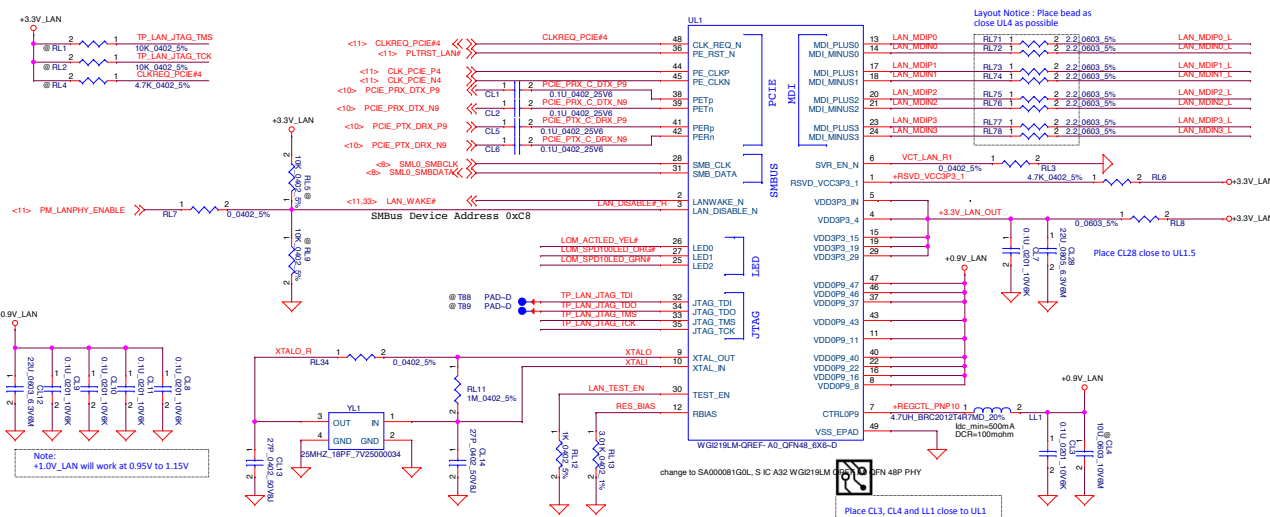
USB 3.0 CONN TYPE C

LA-E121P

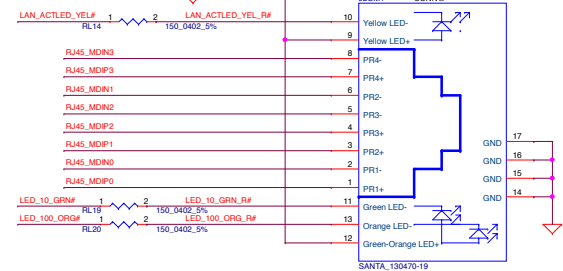
Size	Document Number	Rev
	LA-E121P	0.1
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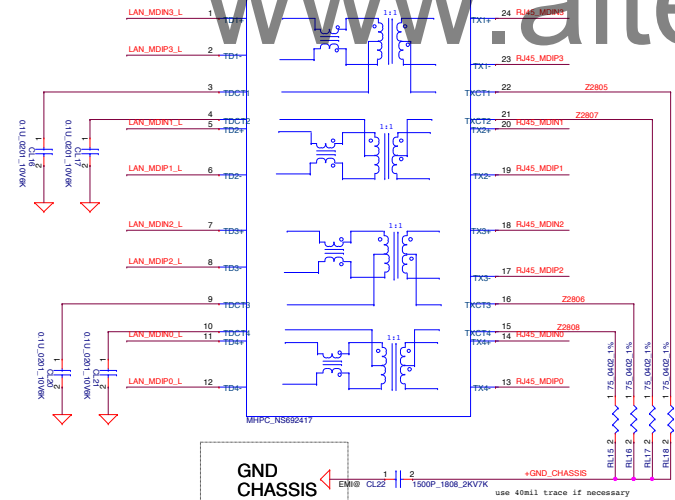
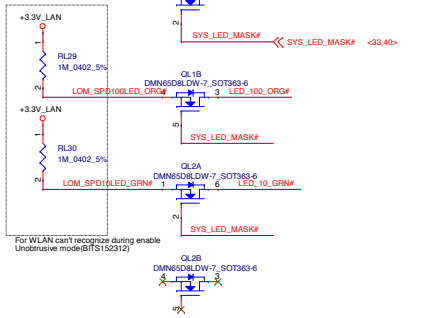
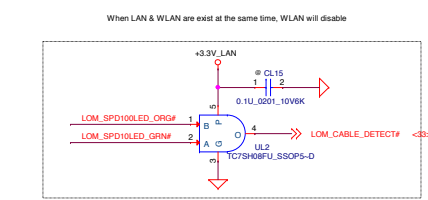
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RJ45 LOM circuit
+3.3V_LAN:20mils



Link DC231603220 (temp) DONE



GND CHASSIS
EM@ CL22 1500P-1808-2KV7K use 40mil trace if necessary

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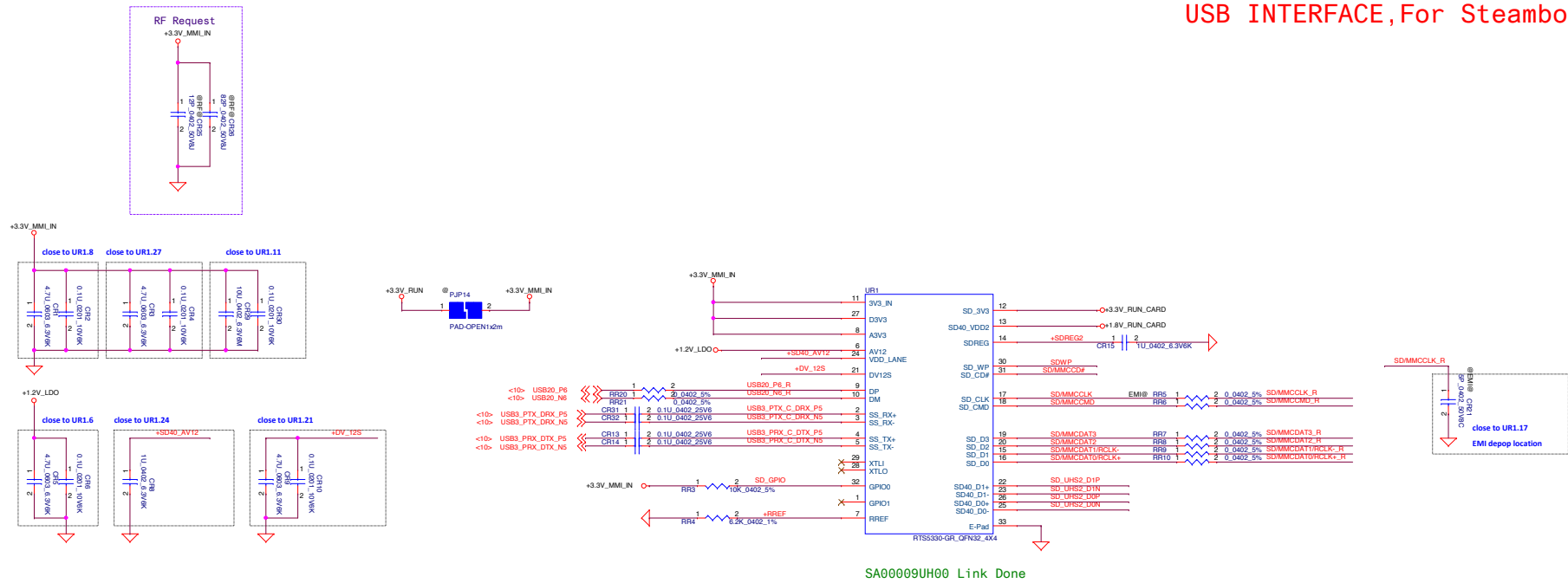
Compal Electronics, Inc.

LAN Clarkville & RJ45

LA-E121P

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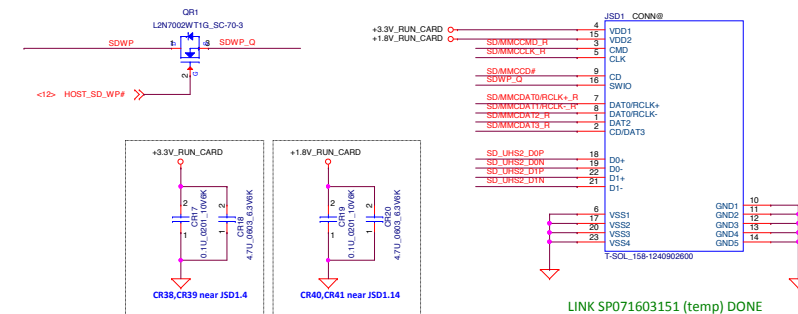
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SA00009UH00 Link Done

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HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)



LINK SP071603151 (temp) DONE

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Card Reader RTS5330

LA-E121P

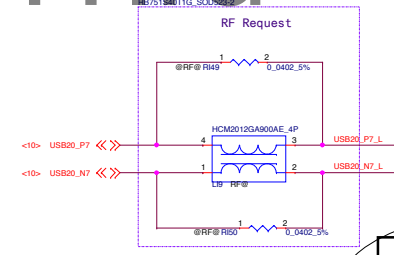
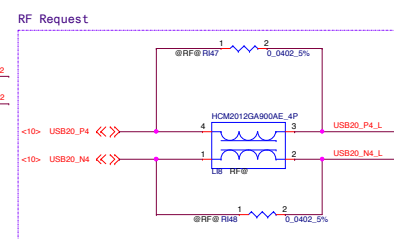
Date: Monday, April 25, 2016 Sheet 30 of 52



for AR Steamboat



SP070019F00 LINK DONE



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCI-E (2 lanes)
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCI-E (1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA



NGFF Card

LA-E121P

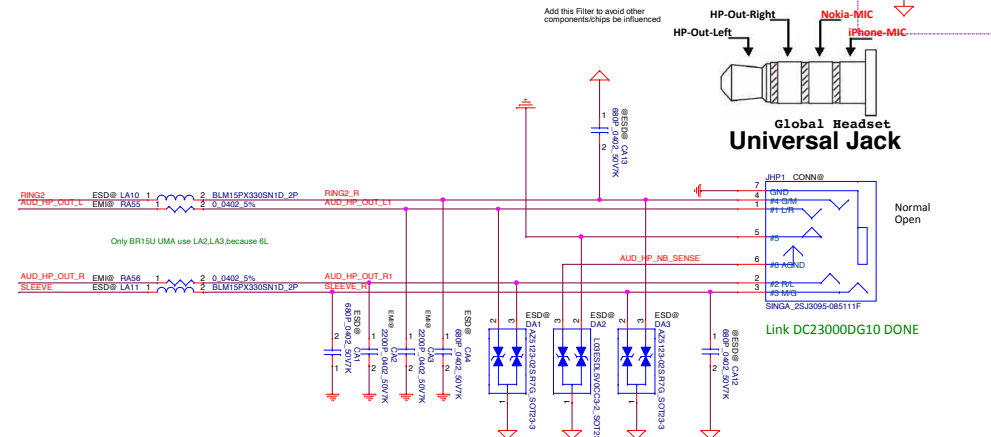
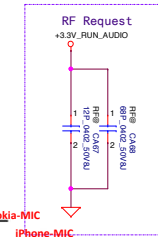
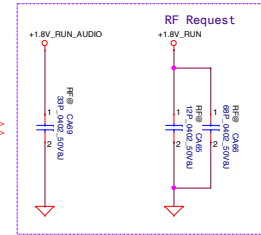
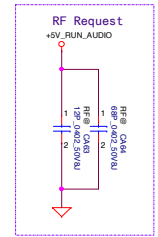
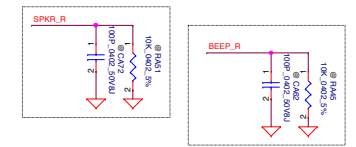
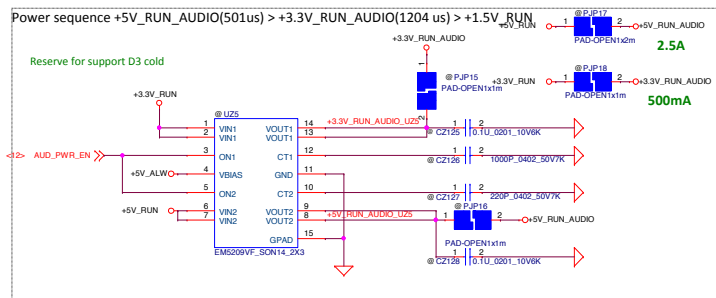
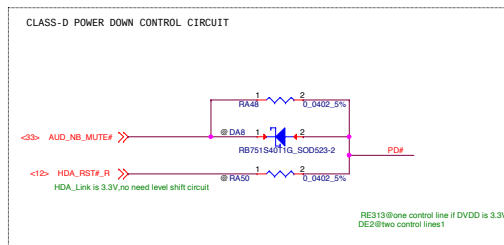
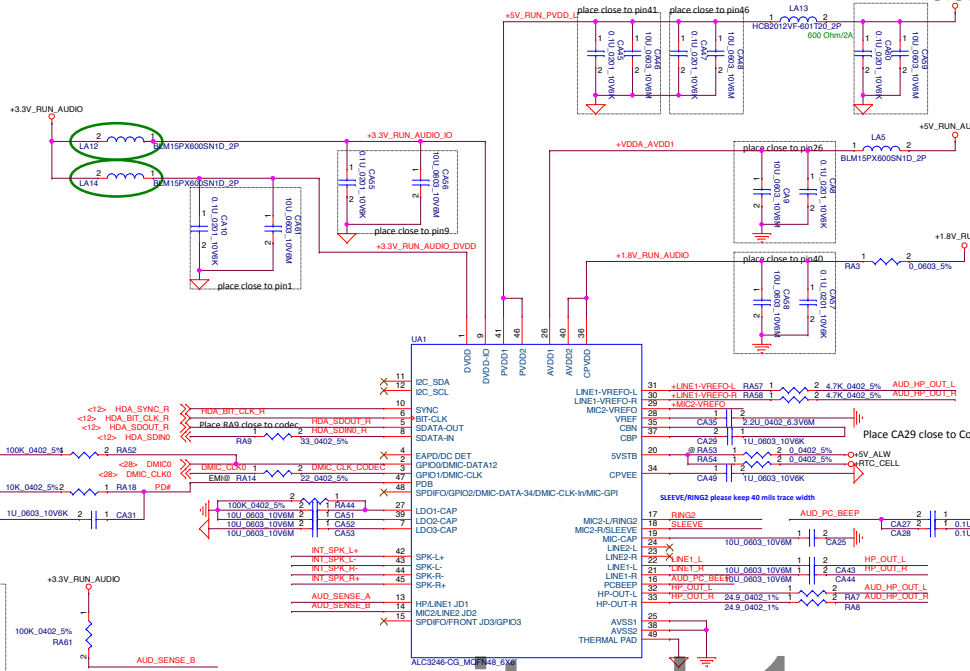
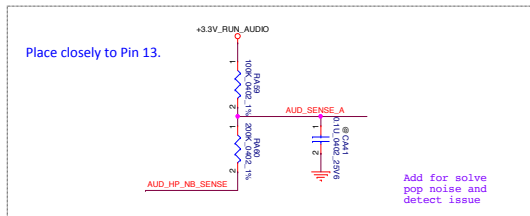
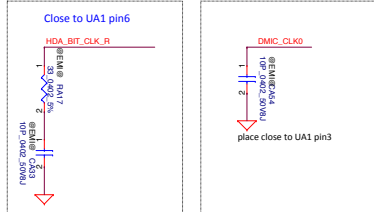
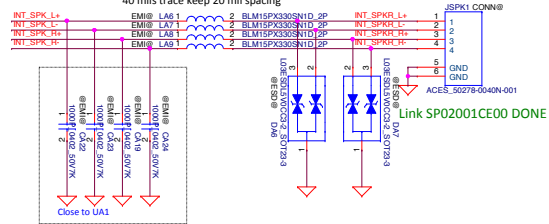
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1W x 1ch, 4ohm (Transducer spec is 80hm/0.5Watt per unit, there are two transducer units in one speaker box)

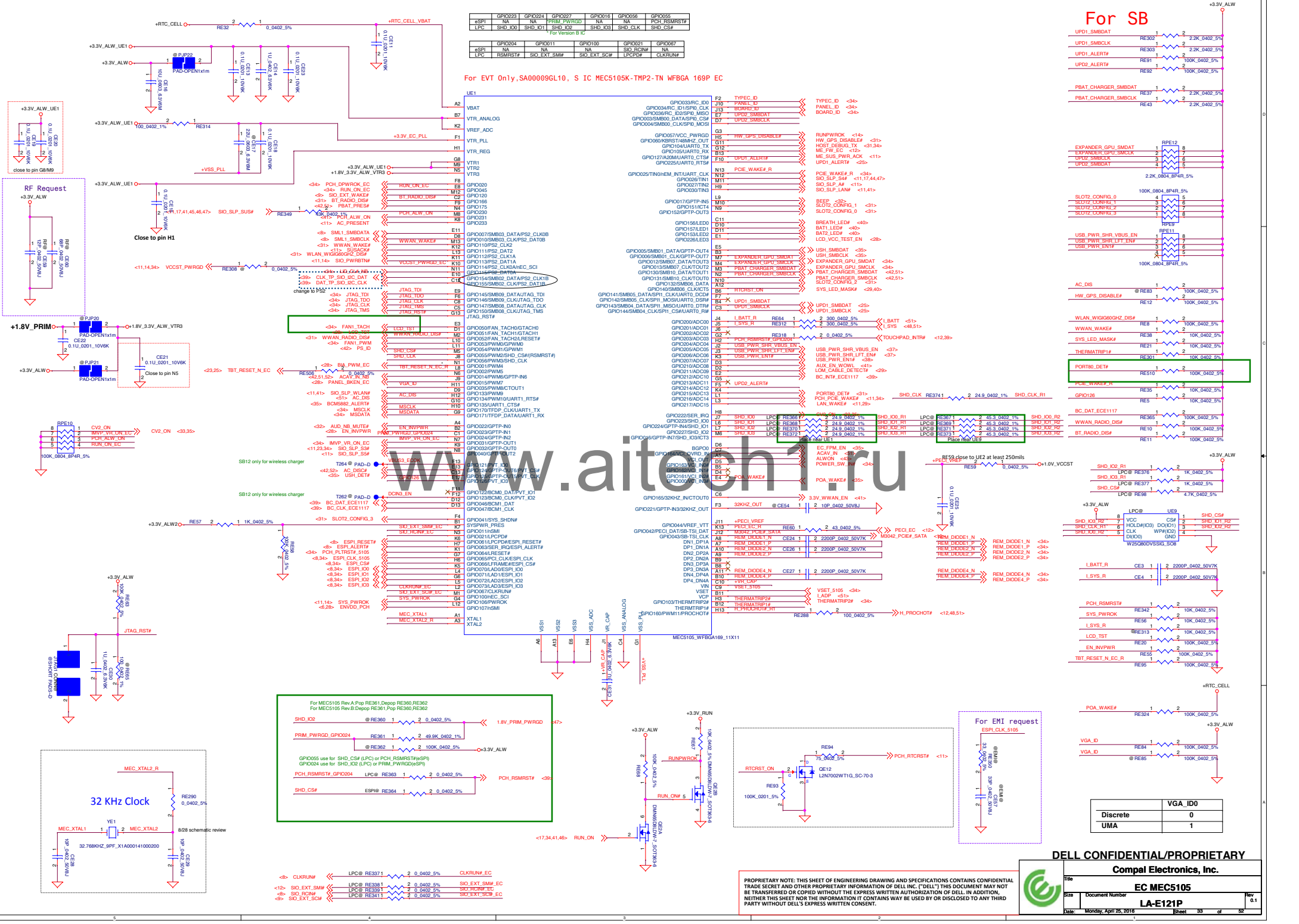
Internal Speakers Header

40 mils trace keep 20 mil spacing

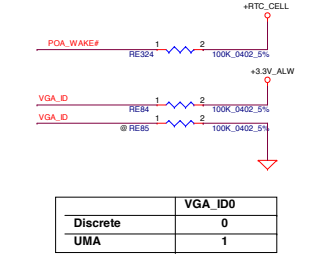
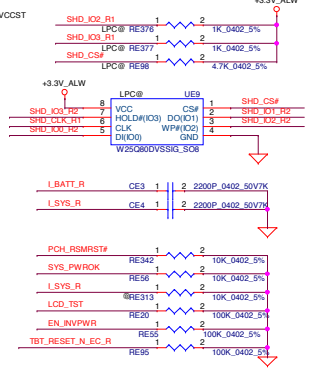
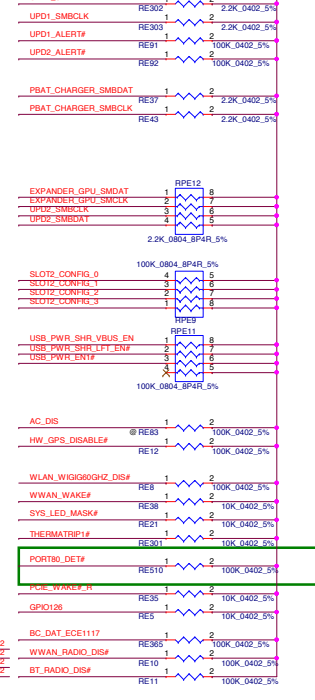


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Issued Date	2016/01/01	Deciphered Date	2017/01/01	
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				Document Number
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				Date
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Codec ALC3246



For SB



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Compal Electronics, Inc.

EC MEC5105

LA-E121P

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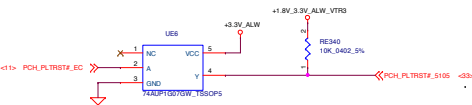
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Discrete 0

UMA 1

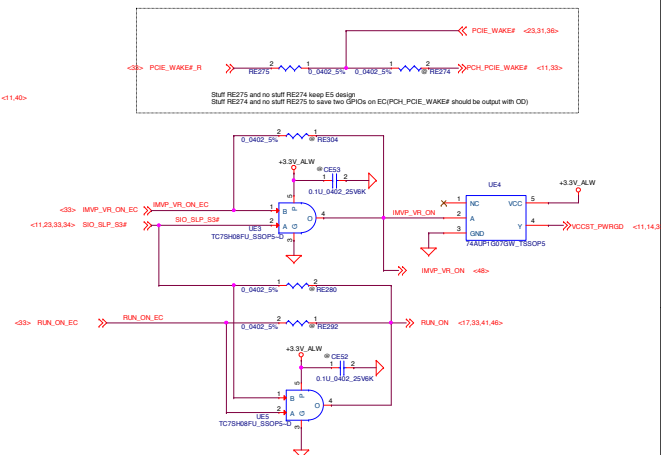
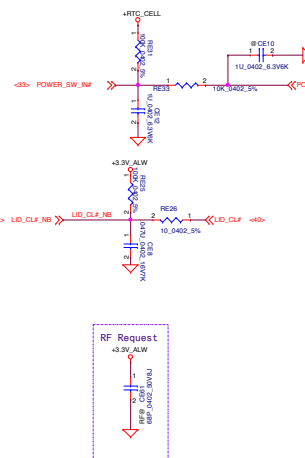
For SB



PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

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RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

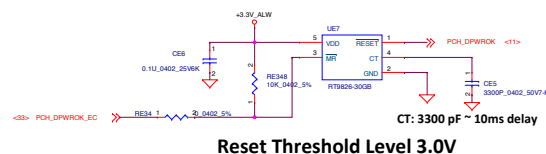
RE79	CE40	REV
240K	4700p	X00
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"

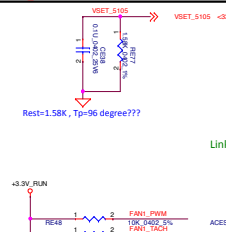
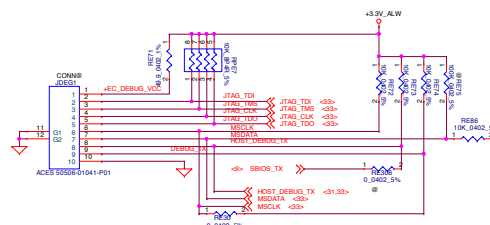
PD ACE_DET# rise time is measured from 5%-68%

BOARD_ID rise time is measured from 5%-68%

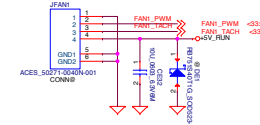
PANEL_ID rise time is measured from 5%-68%



Reset Threshold Level 3.0V

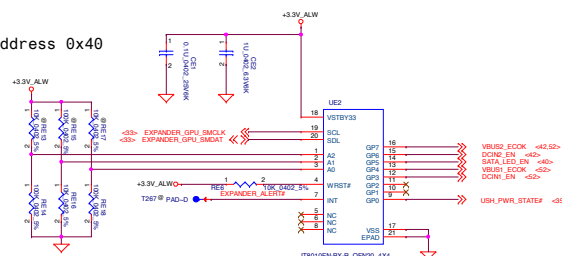


Link 50271-0040N-001 DONE

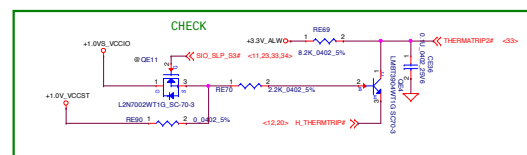


Control Byte
0 1 0 0 A2 A1 A0 R/W
R/W = 0 = Write
R/W = 1 = Read

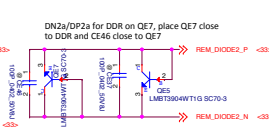
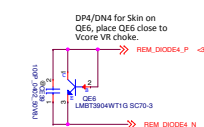
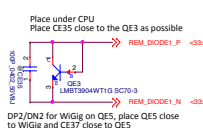
SMBus address 0x40



Link ITE IT8010 SA00009VL00 OK



5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

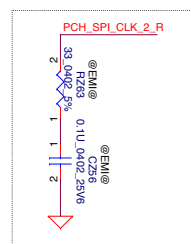
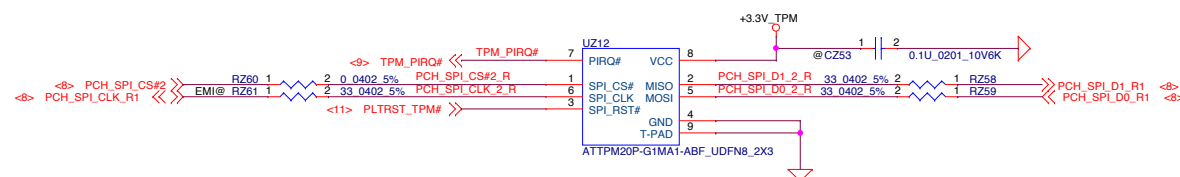
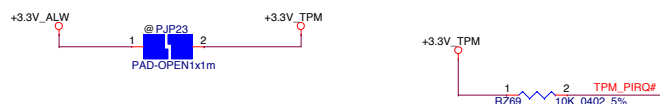
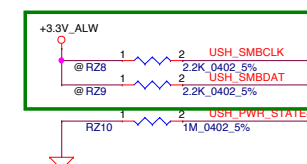
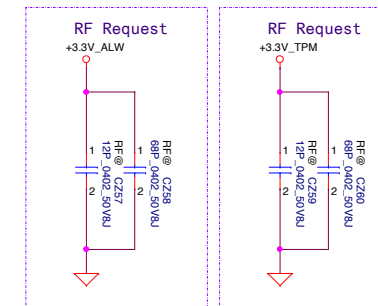


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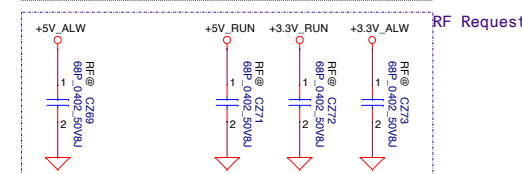
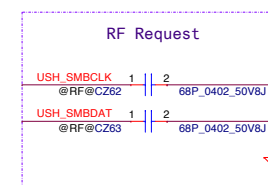
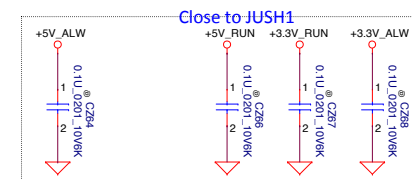
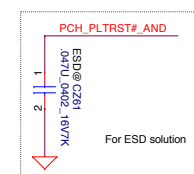
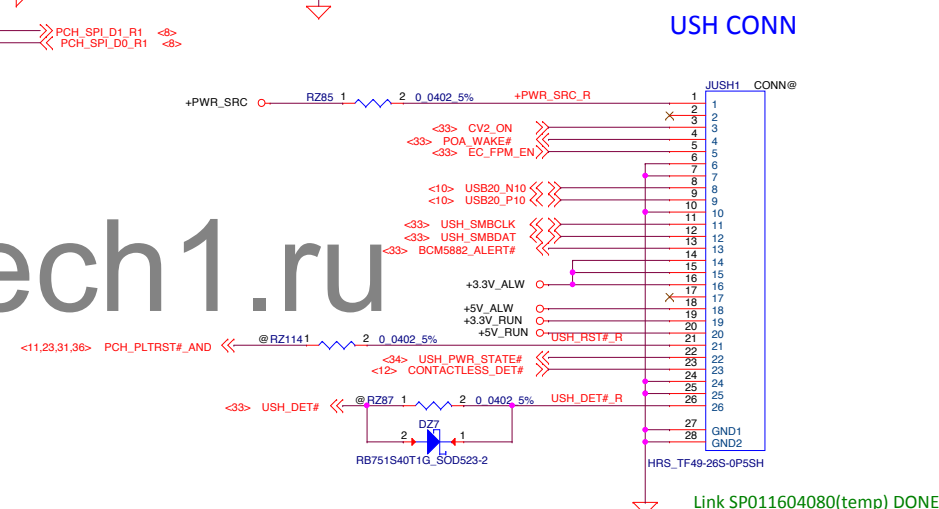
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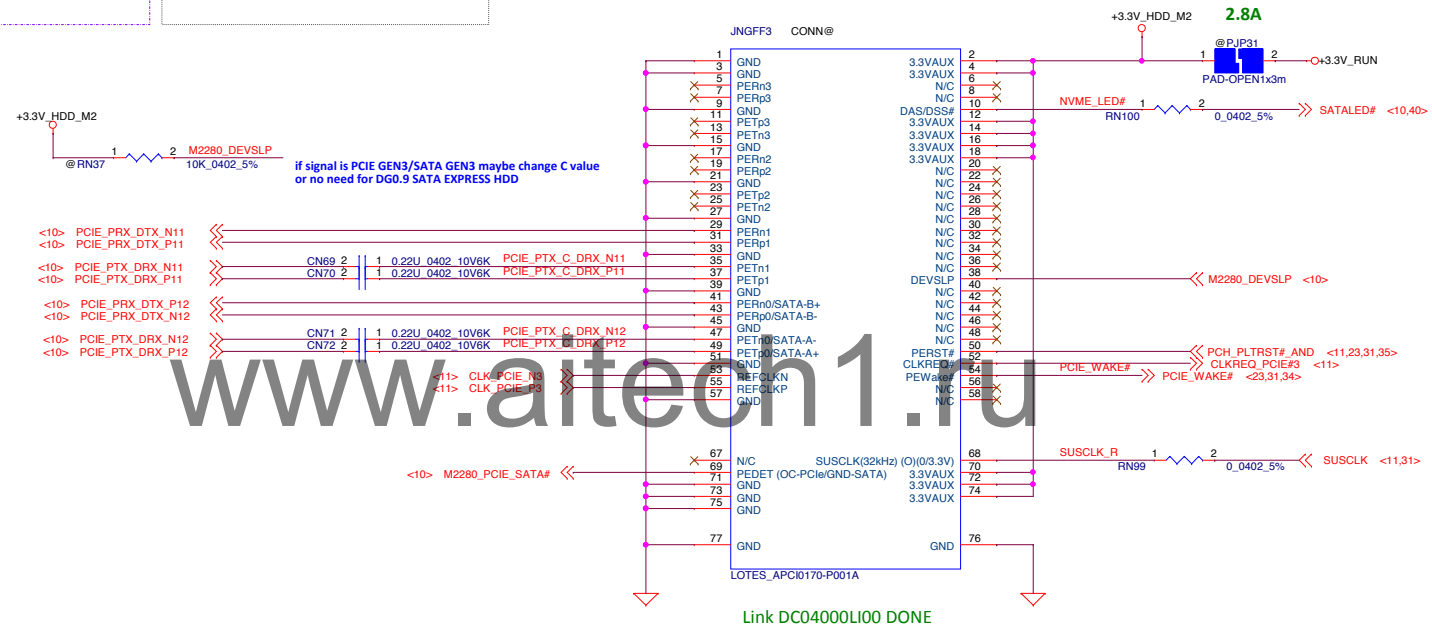
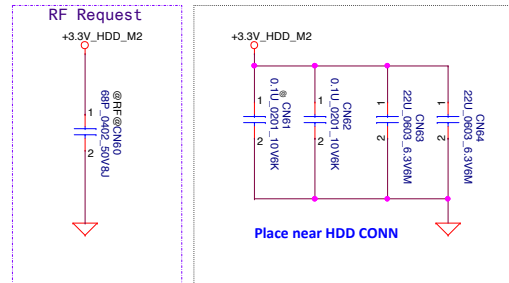
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2280 SSD

NGFF slot C Key M



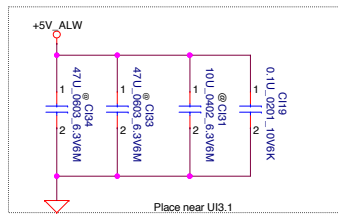
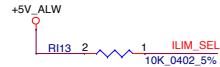
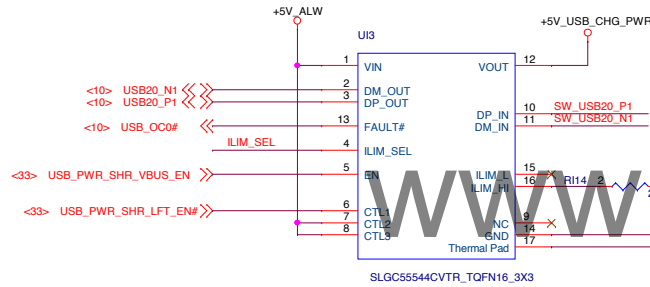
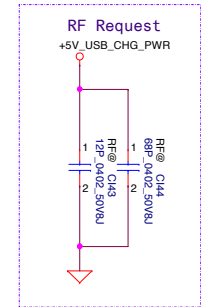
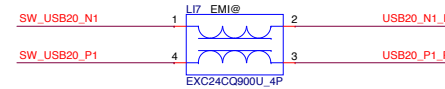
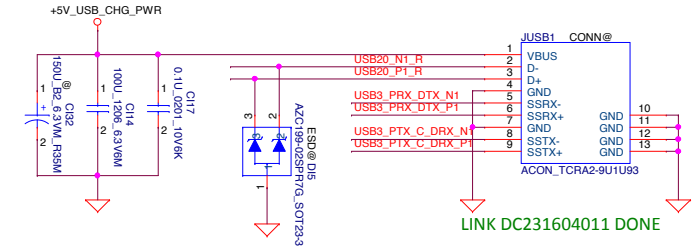
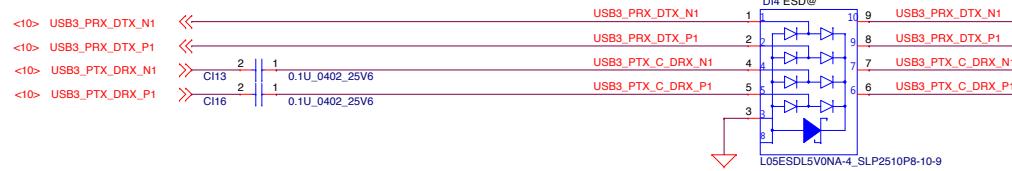
Link DC04000LI00 DONE

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M2 2280 Socket			
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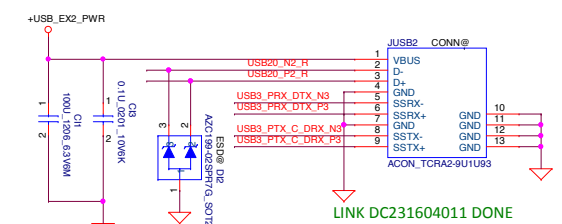
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The diagram shows the USB_PWR_EN1# signal path. It starts with a +5V_ALW supply connected to pin 1 of a 74VHC04 inverter (U11). Pin 2 is connected to ground through a 100nF capacitor and a 100k resistor. Pin 3 is connected to ground through a 0.1uF capacitor and a 100k resistor. The output of the inverter (pin 4) is connected to the USB_OC1# signal line. The inverter is labeled U11 and has a part number of 74VHC04.

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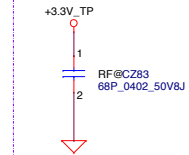
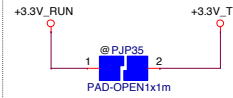
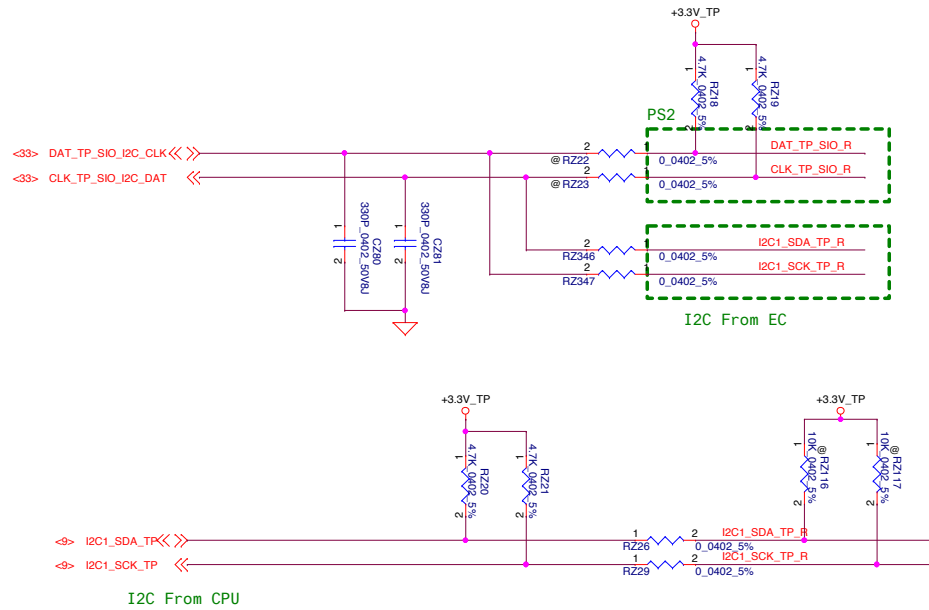
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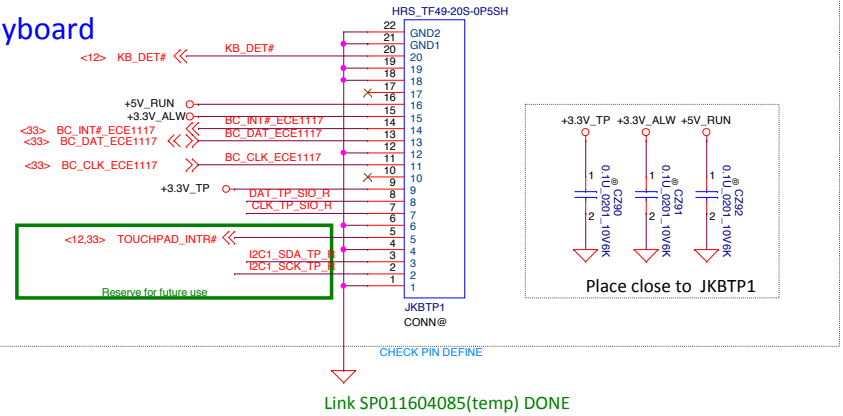
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Touch Pad



Keyboard



@ EDP Cable nonTS_HD/FHD-HD Cam

Part Number	Description
DC02C00E000	H-CONN SET 185 MB-LCD-CAMERA NTS FHD

@ EDP Cable nonTS_FHD-IR

Part Number	Description
DC02C00E100	H-CONN SET 185 MB-LCD-CAMERA-IR NTS FHD

@ EDP Cable TS_TS-FHD-HD Cam

Part Number	Description
DC02C00E200	H-CONN SET 185 MB-LCD-CAMERA-TS FHD

@ LED Cable

Part Number	Description
DC02002L700	H-CONN SET 185 MB-LCD-LED/B

@ FP FFC

Part Number	Description
NBX00023000	FFC 12P F P0.5 PAD=0.3 56MM MB-FP 1S5

@ TP FFC

Part Number	Description
NBX00022Y00	FFC 20P F P0.5 PAD=0.3 92MM MB-TP 1S5

@ USH Board FFC

Part Number	Description
NBX00022Z00	FFC 26P F P0.5 PAD=0.3 81.6MM MB-USH 1S5

@ RTC BATT

Part Number	Description
GC02001D800	BATT CR2032 3V 225MAH PA 5 W/C 30MM

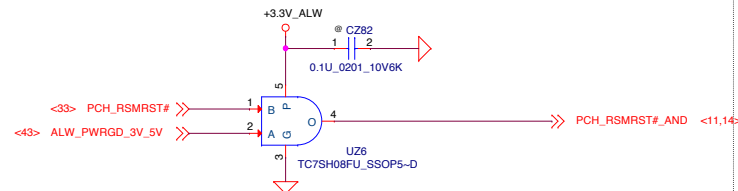
@ FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-BB3 ADDA

@ Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

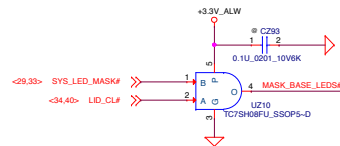
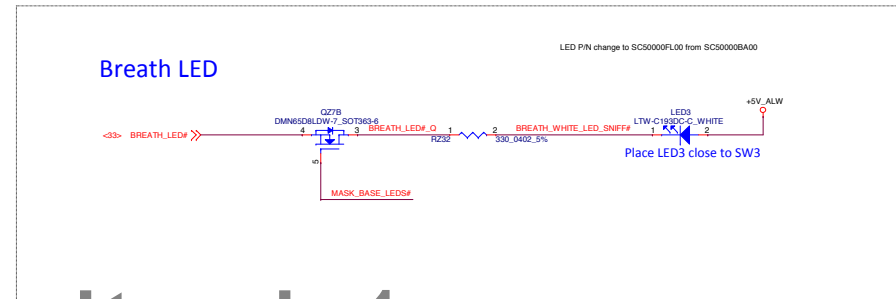
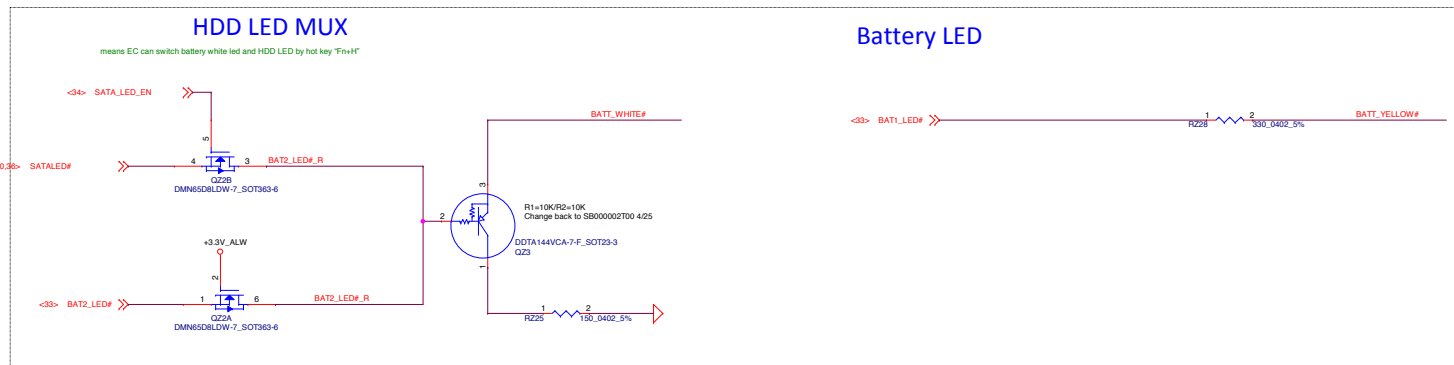
RSMRST circuit



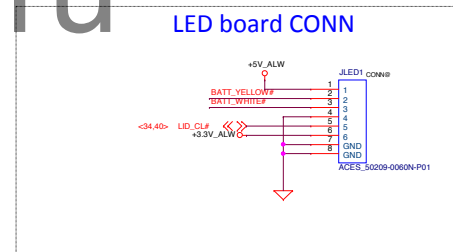
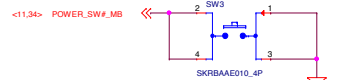
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Keyboard			
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POWER & INSTANT ON SWITCH

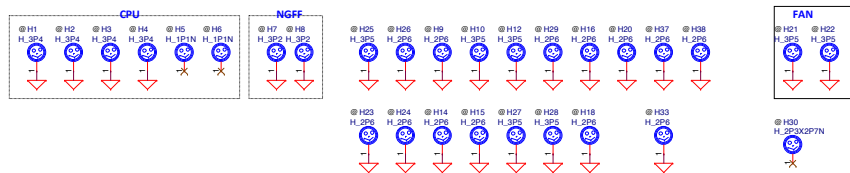


Fiducial Mark



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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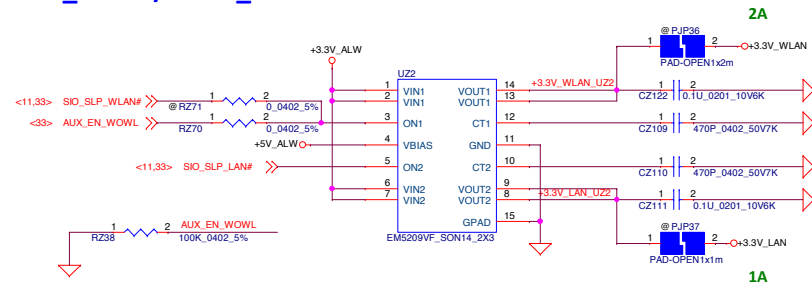
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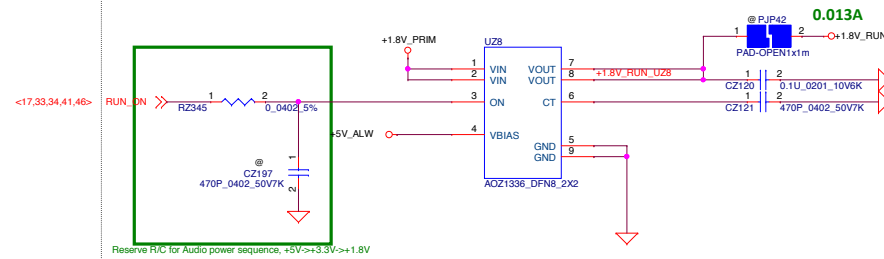
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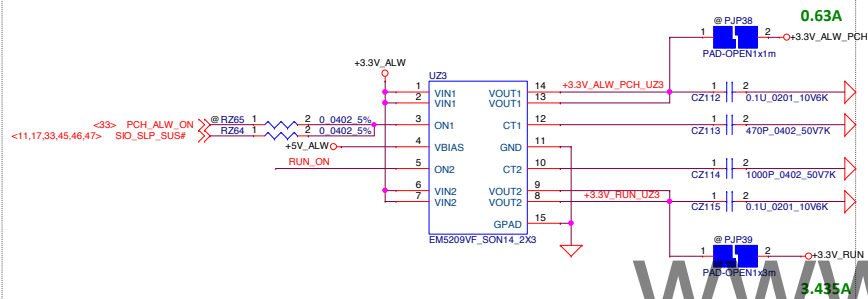
+3.3V_WLAN/+3.3V_LAN source



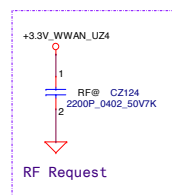
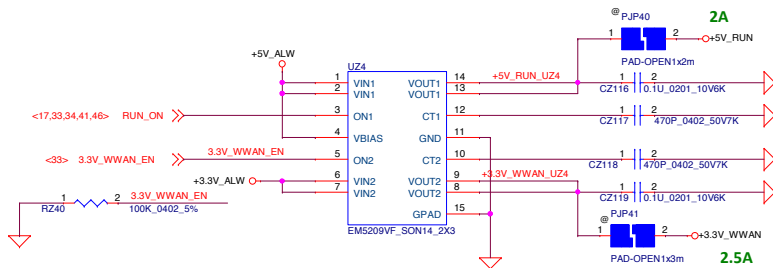
+1.8V_RUN source



+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WWAN source



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Compal Electronics, Inc.

Power control

LA-E121P



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+PWR_SRC

PJP100
PAD-OPEN 1x2m-D

+3.3V_ALW

PGOOD_3V

LX_3V
GND
PG
EN2
EN1
FF
OUT
NC
GND

PU100
LX
IN
IN
IN
IN
BS

LX
GND
PG
EN2
EN1
FF
OUT
NC
GND

LX
GND
PG
EN2
EN1
FF
OUT
NC
GND

LX
GND
PG
EN2
EN1
FF
OUT
NC
GND

LX
GND
PG
EN2
EN1
FF
OUT
NC
GND

LX
GND
PG
EN2
EN1
FF
OUT
NC
GND

LX
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PG
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OUT
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LX
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LX
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OUT
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GND

LX
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PG
EN2
EN1
FF
OUT
NC
GND

LX
GND
PG
EN2
EN1
FF
OUT
NC
GND

+PWR_SRC

PJP101
PAD-OPEN 1x2m-D

+3.3V_ALW

PGOOD_5V

LX_5V
GND
PG
EN2
EN1
FF
OUT
NC
GND

PU102
LX
IN
IN
IN
IN
BS

LX
GND
PG
EN2
EN1
FF
OUT
NC
GND

LX
GND
PG
EN2
EN1
FF
OUT
NC
GND

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PG
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EN1
FF
OUT
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PG
EN2
EN1
FF
OUT
NC
GND

LX
GND
PG
EN2
EN1
FF
OUT
NC
GND

LX
GND
PG
EN2
EN1
FF
OUT
NC
GND

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+3.3V_ALWP

3VALWP
TDC 5.9 A
Peak Current 8.4 A
OCP Current 10.1A

+5V_ALWP

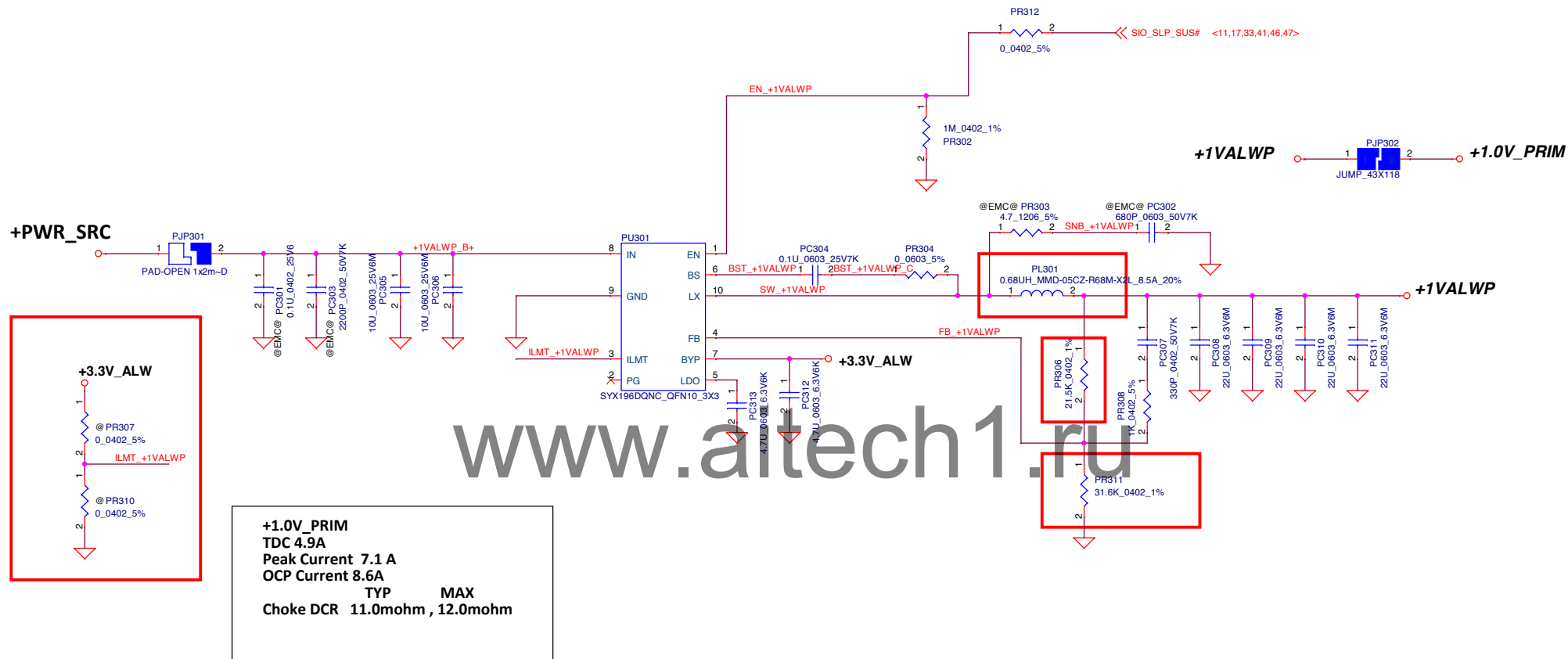
5VALWP
TDC 5.5 A
Peak Current 7.9 A
OCP Current 9.5 A

EN1 and EN2 don't floating

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+5V_ALW/3.3V_ALW			
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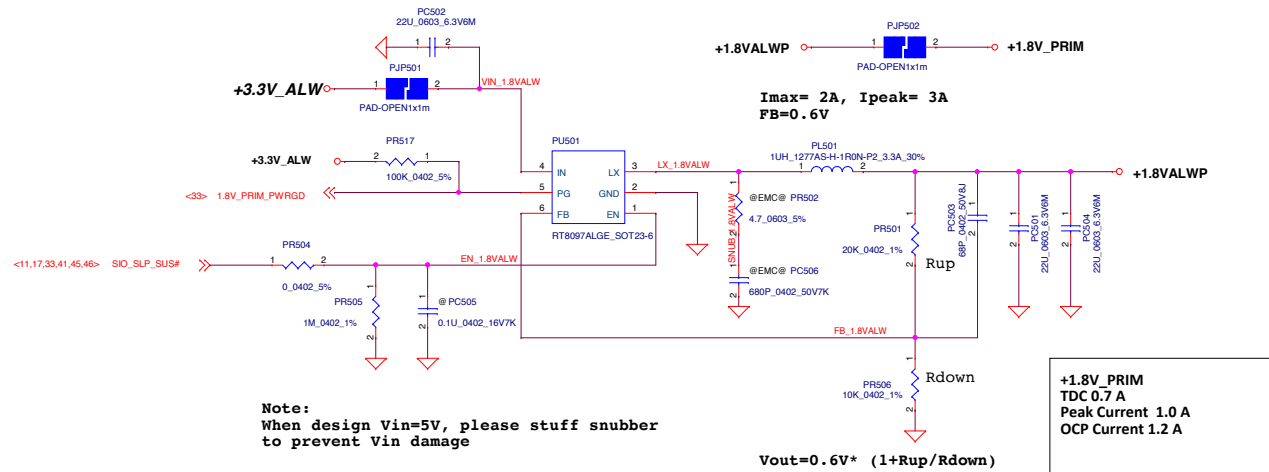


The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

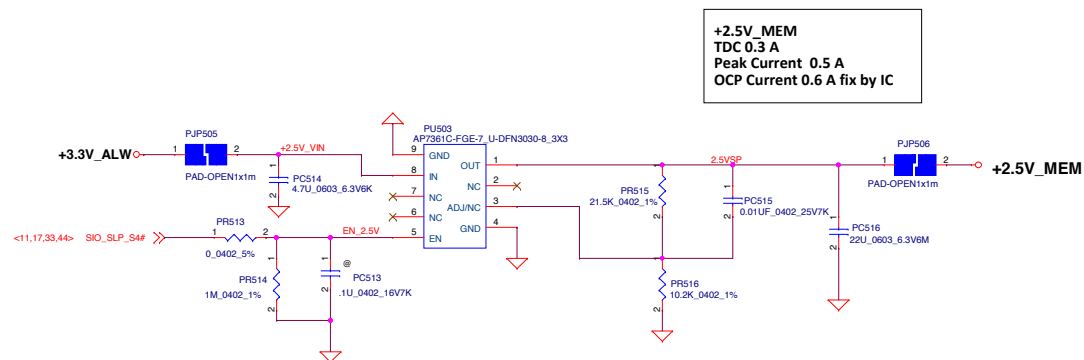
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Title		
+1VALWP		
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		Compal Electronics, Inc.	
		+1.8VALWP/+1.5VSP	
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Local sense put on HW site

+1.0V_VCCST

VCC_SA
TDC 4 A
Peak Current 4.5A
OCP current 5.4A
Choke DCR 13 m ohm

VCCSA_B+ CPU_B+
PAD-OPEN1x1m

VCCSA_B+

+3.3V_RUN

+5V_ALW

+5V_ALW

+VCC_SA

+5V_ALW

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PWR_VCORE_ISL95857

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[illegible]

The diagram illustrates a 16-bit parallel adder implemented using four 4-bit 74181 ALU chips and a 74160 counter. The counter provides addresses for the ALU chips. The ALU chips are configured to perform a 16-bit addition of two 16-bit numbers. The inputs are labeled A[15:0] and B[15:0]. The outputs are labeled S[15:0]. The carry-in is labeled C_in. The carry-out is labeled C_out. The ALU chips are labeled 74181 and the counter is labeled 74160.

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